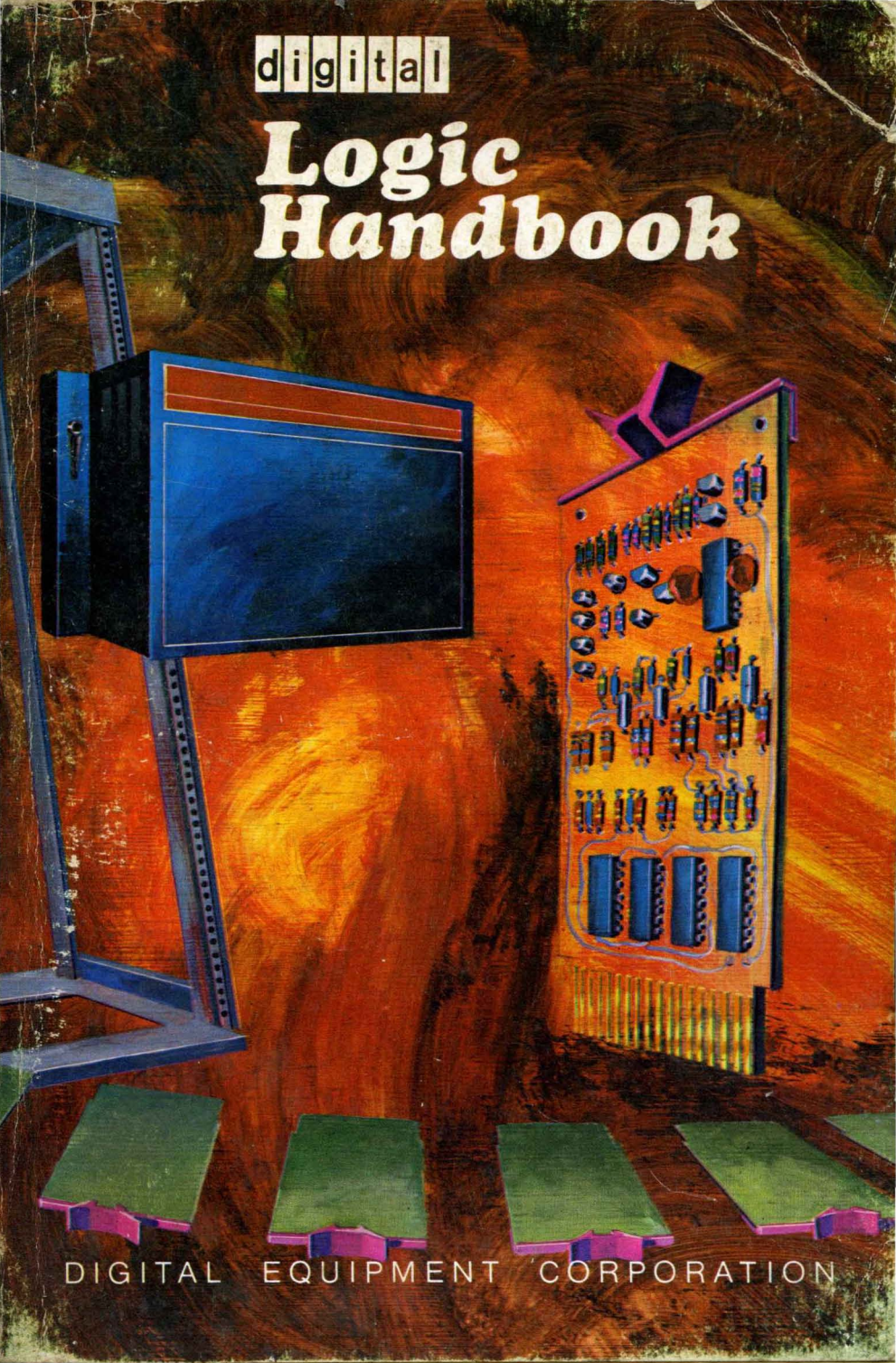
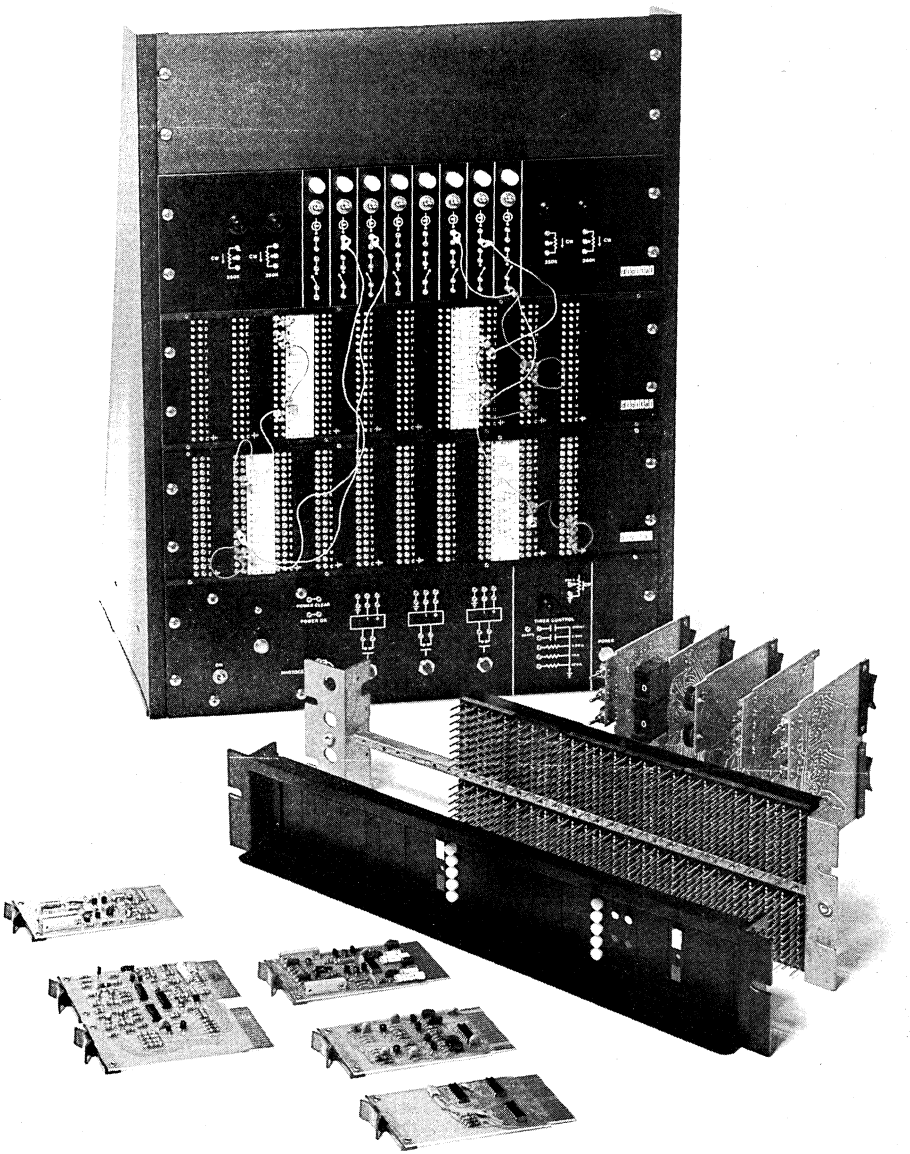
digital

# Logic Handbook



DIGITAL EQUIPMENT CORPORATION



M SERIES

K SERIES

PART I
MODULES

A SERIES

B, R, W SERIES

POWER SUPPLIES

PART II
HARDWARE

HARDWARE

ACCESSORIES

PART III
APPLICATIONS

M SERIES

# THE


# LOGIC HANDBOOK
# FLIP CHIP™ MODULES
# 1970 EDITION

# FOREWORD

This sixth edition of the Logic Handbook is your guide to the most extensive array of logic capabilities, hardware, and applications information ever offered by Digital Equipment Corporation. Here you will find a wealth of useful information on the latest techniques and products available for implementing your electronic logic designs for instrumentation, computer interfacing, data gathering, or control. The handbook is a basic reference for anyone involved in specifying, designing, manufacturing or using solid-state logic.

**The Products**

The M Series TTL integrated circuit modules are featured in this edition. The M Series line has again been expanded and now includes over 85 modules. In addition to this comprehensive array of basic logic and functional logic modules, the general-purpose M Series line also has increased its computer interfacing capabilities. Additions include four new M Series bus interface modules, an input multiplexing module, and an entirely new section on interface modules for the PDP-11.

The K Series product offering has also been expanded. Four new modules are described to bring the total K Series to over 60 modules. A new K Series mounting panel is offered here for the first time. K Series descriptions have been abridged in this edition to provide space to more fully describe the expanded M Series line. However, full and complete descriptions of all K Series modules offered in this book are available in the Control Handbook. Use the handy reply card attached to this book to order your copy. All of the K Series application information plus many new application notes are also available in the Control Handbook.

A complete line of A Series analog-to-digital modules is described here including seven functionally complete digital-to-analog converter modules as well as multiplexer and operational amplifier modules.

An expanded section on Digital's increased wire wrapping capabilities is included in this edition. This section not only simplifies the procedure for using our wire wrap capabilities but also announces new reduced prices for the service.

In this edition, also, is a complete description of the K Series Logic Lab — a device designed for use with K Series modules for building prototype systems and as an effective tool for learning solid-state control logic.

This edition of the Handbook includes an abridged section on all of our major negative logic modules . . . the R, B, and W Series.

These module descriptions will be of particular importance to designers who are preparing interfaces to most of Digital's negative bus computers such as the PDP-9 and 8 families.

As the cost of the basic logic itself decreases, it becomes increasingly important that efficient, reliable, and inexpensive hardware be available to keep total system costs down. Digital provides this hardware. Now, from a few to thousands of modules can be connected, wired, mounted, powered, and enclosed efficiently at the lowest cost per function in the industry.

Digital's complete line of power and hardware accessories provides everything needed to put your designs into action, from connector blocks to mounting cabinets. Power supplies, connector block variations, mounting panels, blank module configurations, connector cards and a complete line of computer-grade cabinetry are among the well over 100 different hardware, power, and accessory items described in this edition of the Logic Handbook.

Seven complete M Series applications notes and dozens of useful design notes have been included to help you easily design custom systems making this one of the most informative electronic handbooks available.

**The Company**

In a little over twelve years, Digital has become a major force in the electronics industry. The company has grown from three employees and 8,500 square feet of production floor space in a converted woolen mill in Maynard, Massachusetts, to an international corporation employing more than 5,000 people with well over one million square feet of floor space in a dozen manufacturing, sales, and service facilities around the world. In addition to the corporate headquarters in Maynard, other Massachusetts manufacturing facilities are located in Westfield, Westminster, and Leominster. Internationally, Digital has manufacturing plants in Puerto Rico, England, and Canada.

From its beginnings as a manufacturer of digital modules, the company has now grown to the point where it is the world's largest manufacturing supplier of logic modules and the third largest computer manufacturer, by number of installations, in the industry. Digital's rise as a leader in the electronics industry began in 1957 with the introduction of the company's line of electronic circuit modules. These solid-state modules were used to build and test other manufacturers' computers. A year later, Digital introduced its first computer, the PDP-1. The PDP-1 heralded a new concept for the industry — the small, on-line computer. And the PDP-1 was inexpensive — it sold for $120,000 while competitive machines with similar capabilities were selling at over $1 million. But the PDP-1 was more than a data processor; more than just a tool to manipulate data. It was a system that could be connected to all types of instrumentation and equipment for on-line, real-time monitoring, control, and analysis. It was a system with which people and machines could interact.

Also, in 1958, Digital introduced the Systems Modules, high-quality, low-cost solid-state digital logic circuits on a single printed circuit card. Today, electronic modules like the ones Digital introduced are used in most electronic equipment, from computers to television sets.

In 1965, Digital announced the first of the FLIP CHIP module lines. These highly reliable modules include cards for internal computer logic, interfacing, control and analog-to-digital conversion.

About two years ago, Digital announced the newest additions to the FLIP CHIP family: M Series high-speed integrated circuit modules and K Series noise-immune modules. Last year, Digital introduced the PDP-1's grandson, the PDP-8/L. It is a smaller computer with far greater capabilities than the PDP-1 and a price tag of only $8,500. Also last year, Digital announced the PDP-14 — a solid-state repetitive controller, designed specifically for industrial machine control.

This year, Digital introduced a new line of computers, the PDP-11, which complements Digital's other two small computer lines, the PDP-8 and PDP-12. The PDP-11's modular construction and the Unibus concept make it unique.

Digital produces over two million modules a year, making it the world's largest manufacturing supplier of logic modules. Digital's sales engineers in over 60 offices around the world and applications engineering staff at the home office are ready to help you with your most difficult or complex applications. They are all listed on the inside back cover. Give us a call.

**ACKNOWLEDGEMENTS**

It is impossible to properly acknowledge the efforts of the hundreds of individuals involved in writing and producing a Handbook of this complexity. A few individuals, however, deserve to be singled out. Among those are John Bloem and Joe Orlando who spent many long days preparing the technical information for this Handbook as well as checking innumerable pages of typeset. Also, the production assistance of Frank Coco and the editorial help of Gabe Del Rossi deserve to be acknowledged. The cover for this Handbook is an original design conceived and executed by Norm Gardner of Boston.

March, 1970

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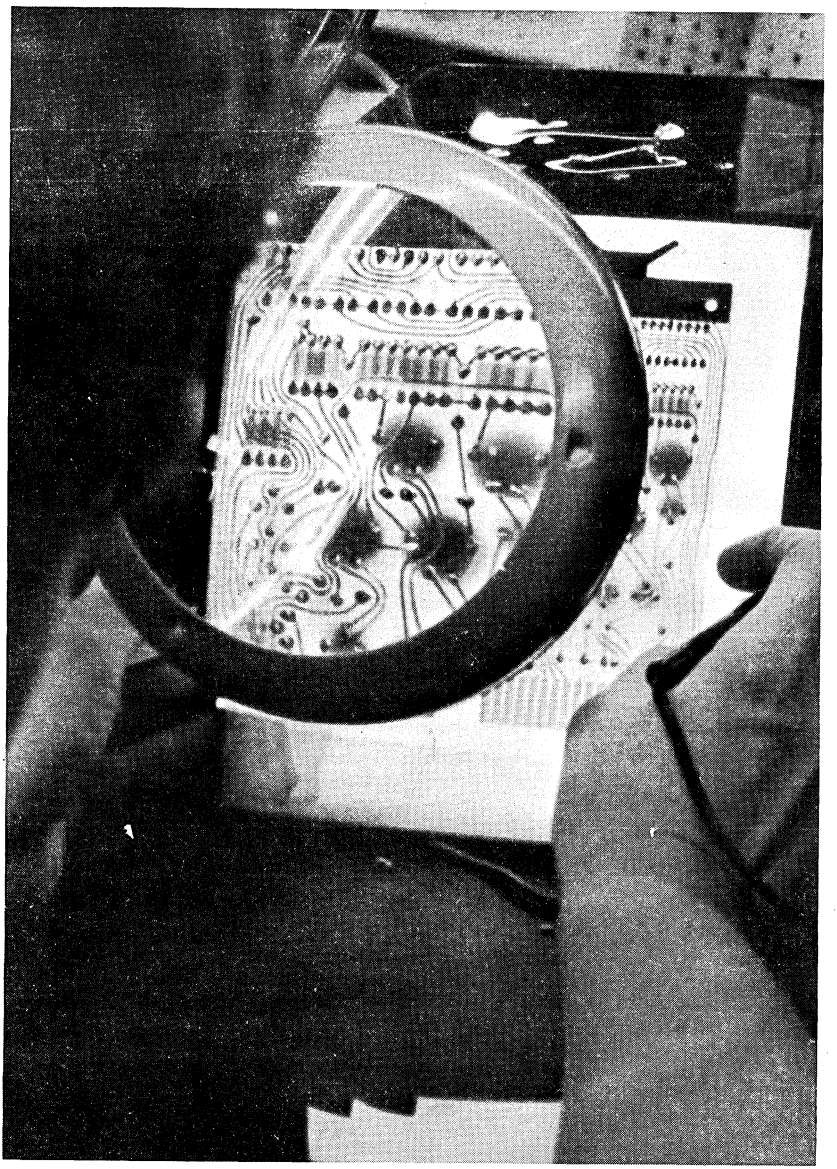


DEC Module assembly lines combine automated manufacturing steps with visual inspection and computer controlled testing.

# PART I
# M
# SERIES

# INTRODUCTION

The development of monolithic integrated circuits has had an impact on the design of digital module systems. Advantages of small size and high operating speeds made these circuits initially attractive. However, a lower price/performance ratio compared to hybrid or discrete component modules offset the advantages. Recently, significant price reductions in both TTL (transistor-transistor logic) and DTL (diode-transistor logic) integrated circuits indicated a re-evaluation was needed.

DIGITAL EQUIPMENT CORPORATION undertook a study of both types of logic, their performance in large and small systems, and their ease of use in system design. The result of this study is the M Series Integrated Circuit FLIP CHIP™ Module.

M Series modules contain high speed TTL logic in both general purpose and functional logic arrays. TTL was chosen for its high speed, capacitance drive capability, high noise immunity and choice of logical elements. High performance integrated circuit modules are now available at approximately one half the price of their discrete or hybrid counterparts.

In addition to the reduced cost of integrated circuits, Digital's advanced manufacturing methods and computer controlled module testing have resulted in considerable production cost savings, reflected in the low price of all M Series Modules.

# GENERAL CHARACTERISTICS

M Series high-speed, monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) integrated circuits which provide high speed, high fan out, large capacitance drive capability and excellent noise margins. The M Series includes a full digital system complement of basic modules which are designed with sufficient margin for reliable system operation at frequencies up to 6 MHz. Specific modules may be operated at frequencies up to 10 MHz. The integrated circuits are dual in-line packages.

The M Series printed circuit boards are identical in size to the standard FLIP CHIP™ modules. The printed circuit board material is double-sided providing 36-pins in a single height module. Mounting panels (H910 and H911) and 36-pin sockets (H803 and H808) are available for use with M Series modules. Additional information concerning applicable hardware may be found in the Power Supply & Hardware and Accessories section of this handbook.

M Series modules are compatible with Digital's K Series and, through the use of level converters, are compatible with all of Digital's other standard negative voltage logic FLIP CHIP™ modules.

## TTL NAND GATE

The basic gate of the M Series is a TTL NAND GATE. Figure 1 is the basic two input NAND gate schematic diagram. The circuit is divided into 3 major sections, the multiple emitter input, the phase splitter and the totem pole output circuit. The two diode model of a transistor shown in Figure 2 will be used in the analysis of the circuit. A forward biased silicon junction (i.e. diode) gives a voltage drop of about 0.75 volts and a saturated silicon transistor has a collector emitter voltage of 0.4 volts average. These two figures will be used throughout the following discussion.

With either input at the LO logic level (0.0V-0.8V) the multiple emitter input transistor will be ON with its base residing at about 0.75 + 0.4 = 1.15 volts. The three diode string consisting of $Q_1$'s base collector diode, $Q_2$'s base emitter diode, and $Q_4$'s base emitter diode will have only 1.15 volts across it and will therefore be conducting only leakage currents (0.75 + 0.75 + 0.75 = 2.25 volts required for forward bias). With no current flowing into the base emitter junction of $Q_2$, the transistor will be OFF and its collector emitter voltage is alowed to rise. Similarly with no current flowing in the base emitter diode of $Q_4$ the transistor is OFF and its collector emitter voltage is allowed to rise. When both $Q_2$ and $Q_4$ are OFF, $Q_3$ is freed to pull the output voltage to a HI level. The voltage levels present in the circuit with one or more LO inputs is shown in Figure 4.

If both inputs are HI (2.4-3.6 volts) the head of the three diode string will reside at about 2.25 volts and there will be a current path from the 4K base resistor on the input transistor through the diode string to ground as shown in Figure 5. With current flowing in the base emitter junctions of both $Q_2$ and $Q_4$, both transistors will be turned ON. $Q_3$ is held OFF whenever $Q_2$ is ON. The output is driven LO (0.0V-0.4V) by transistor $Q_4$. The voltage levels present in the circuit with both inputs HI and are shown in Figure 6.

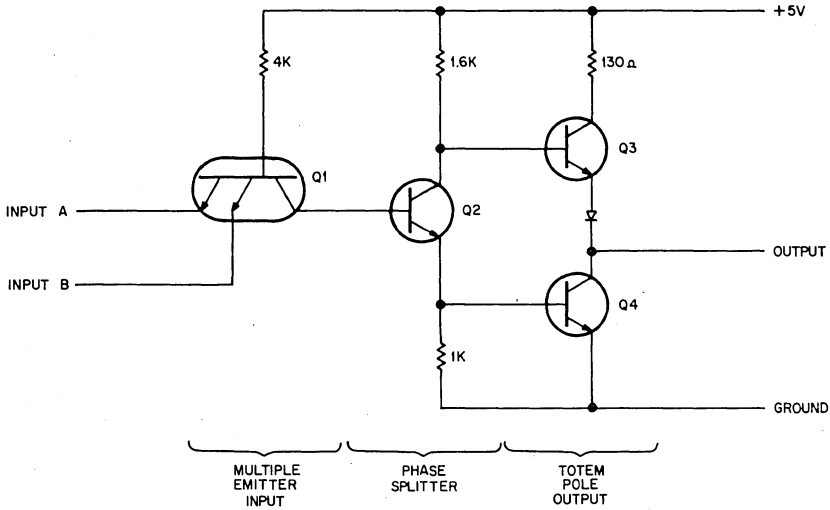



Figure 1 TTL NAND Gate Schematic Diagram

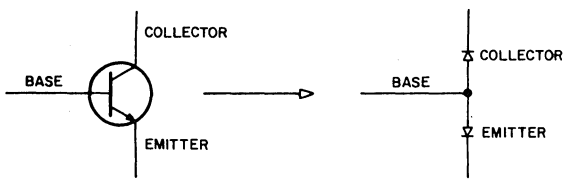



Figure 2 Two Diode Model For Transistor

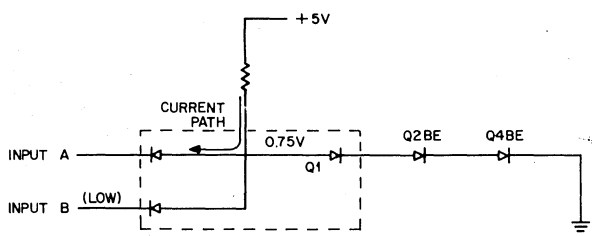



Figure 3 Diode Equivalent NAND Gate Circuit. One Input LO

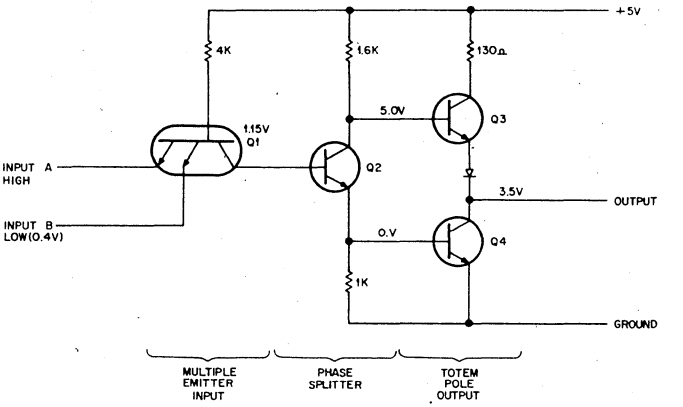



Figure 4 TTL NAND Gate Schematic Diagram, One Input LO

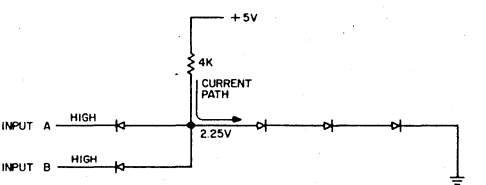



Figure 5 Diode Equivalent NAND Gate Circuit, Both Inputs HI

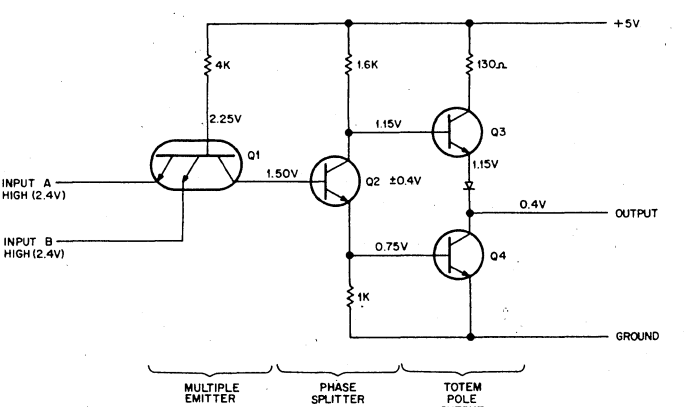



Figure 6 TTL NAND Gate Schematic Diagram, Both Inputs HI

## OPERATING CHARACTERISTICS

**Power Supply Voltage:** 5 volts ± 5%

**Operating Temperature Range:** 0° to 70°C

**Speed:** M Series integrated circuit modules are rated for operation in a system environment at frequencies up to 6 MHz. Specific modules may be operated at higher frequencies as indicated by the individual module specifications.

**LOGIC LEVELS AND NOISE MARGIN**

A gate input will recognize 0.0 volts to 0.8 volts as logical LO and 2.0 volts to 3.6 volts will be recognized as a logical HI. An output is between 0.0 volts and 0.4 volts in the logical LO condition. The logical HI output condition is between 2.4 volts and 3.6 volts. Figure 7 shows diagrammatically the acceptable transistor-transistor logic levels. The worst case noise margin is 400 millivolts that is, an output would have to make at least a 400 millivolt excursion to cause an input which is connected to it to go into the indetermined voltage region. For instance if an output were at 0.4 volts (worst case logical LO) there would have to be a + 400 mv swing in voltage to cause inputs connected to it to go into their indetermined region.

**Input and Output Loading:** The input loading and output drive capability of M Series modules are specified in terms of a specific number of unit loads. Typically the input loading is one unit, however certain modules may contain inputs which will present greater than one unit load. The typical M Series module output will supply 10 unit loads of input loading. However, certain module outputs will deviate from a 10 unit load capability and provide more or less drive. Always refer to the individual module specifications to ascertain actual loading figures.

**Unit Load:** In the logic O state, one unit load requires that the driver be able to sink 1.6 milliamps (maximum) from the load's input circuit while maintaining an output voltage of equal to or less than +0.4 volts. In the logic 1 state, one unit load requires that the driver supply a leakage current 40 microamps (maximum) while maintaining an output voltage of equal to or greater than +2.4 volts.

**Timing:** M Series pulse sources provide sufficient pulse duration to trigger any M Series flip-flop operating within maximum propagation delay specifications. Detailed timing information appears later in this section and in the module specifications.

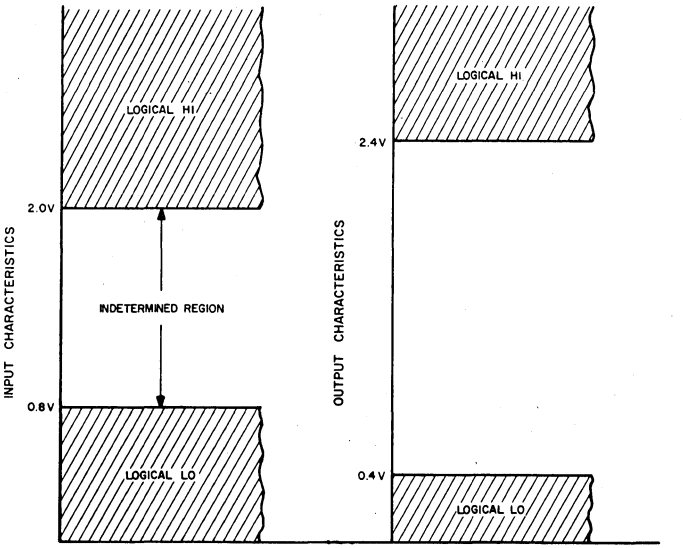
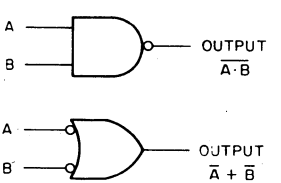



Figure 7 Logic Levels

**NAND Logic Symbol:** Logic symbology used to describe M Series modules is based on widely accepted standards. Logic symbols and a truth table for the NAND gate are shown in Figure 8.




| A | B | OUTPUT |
|---|---|---|
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

Figure 8 NAND Gate Logic Symbol and Truth Table

The first symbol is visually more effective in applications where two high inputs are ANDed to produce a low output. The second symbol better represents an application where low inputs are ORed to produce a high output.

## TTL AND/NOR GATE

With a few modifications, the basic TTL NAND gate can perform an AND/NOR function useful in exclusive OR, coincidence, line selection and NOR gating operations. The modified circuit is shown in simplified form in Figure 9.

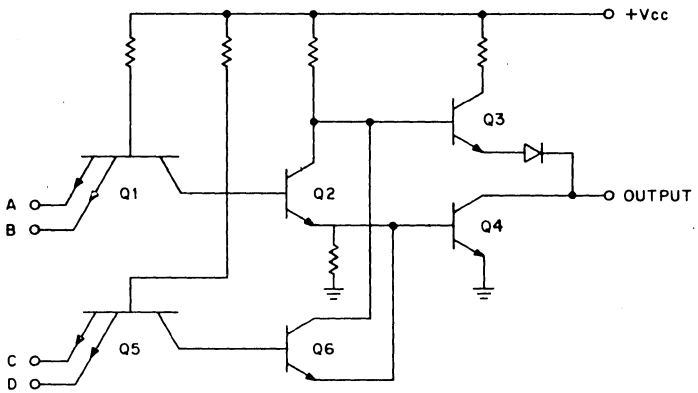
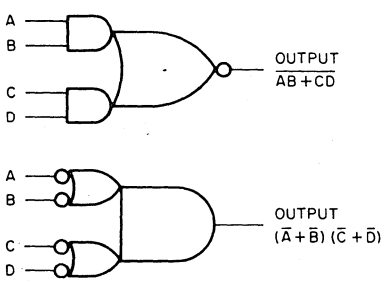



Figure 9 TTL AND/NOR Gate Simplified Schematic

**Circuit Operation:** The basic elements of the TTL NAND gate are used without modification. The phase-splitter (Q2) is paralleled with an identical transistor (Q6), also controlled by multiple-emitter input transistor which receives two additional inputs, C and D. When either of the input pairs are high, the phase inverter operates to switch the output voltage low. Circuit performance is essentially identical to the TTL NAND circuit.

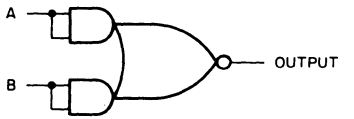
**AND/NOR** Logic Symbol: The logic symbols for the AND/NOR gate are shown and defined in Figure 10.



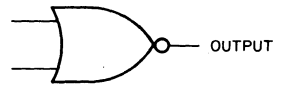

| A | B | C | D | OUTPUT |
|---|---|---|---|---|
| H | H | ANY | | L |
| ANY | | H | H | |
| L | H | L | H | H |
| L | H | H | L | |
| H | L | H | L | |
| H | L | L | H | |

Figure 10 AND/NOR Gate Logic Symbols and Truth Table

**NOR Configuration:** The AND/NOR gate can perform a straight NOR function if the AND gate inputs are tied together as shown in Figure 11.




AND/NOR INPUTS TIED

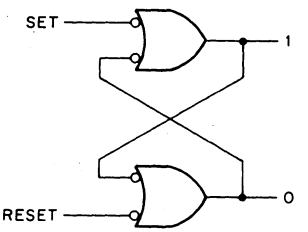



RESULTING NOR SYMBOL

Figure 11 NOR Connection of AND/NOR Gate

**NAND GATE FLIP-FLOPS**

**RS Flip-Flop:** A basic Reset/Set flip-flop can be constructed by connecting two NAND gates as shown in Figure 12.




| PREVIOUS STATE | | INPUT CONDITION | | RESULT | |
|---|---|---|---|---|---|
| 1 | 0 | SET | RESET | 1 | 0 |
| L | H | L | H | H | L |
| H | L | H | L | L | H |
| L | H | H | H | NO CHANGE | |
| H | L | H | H | NO CHANGE | |
| H | L | L | H | NO CHANGE | |
| L | H | H | L | NO CHANGE | |
| L | H | L | L | H | H* |
| H | L | L | L | H | H* |

Ambiguous state: In practice the input that stays low longest will assume control.

Figure 12 RESET/SET NAND Gate Flip-Flop

**CLOCKED NAND GATE FLIP-FLOPS**

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs. (See Figure 13.) One of the inputs of each NAND is tied to a common clock or trigger line.

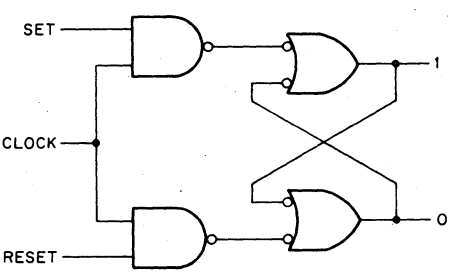



Figure 13 Clocked NAND Gate Flip-Flop

A change of state is inhibited until a positive clock pulse is applied. The ambiguous case will result if both the set and reset inputs are high when the clock pulse occurs.

**M SERIES GENERAL-PURPOSE FLIP-FLOPS**

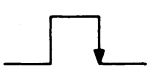
Two types of general-purpose flip-flops are available in the M Series, both of which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.

**FLIP-FLOP CLOCK INPUT SYMBOLS**

The D type flip-flop is a true leading (positive going voltage) edge triggered flip-flop and the D input is locked out until the clock input returns to low. The symbol to indicate this function will be as follows;

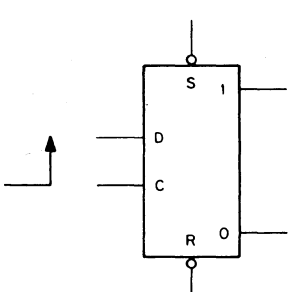
D TYPE FLIP FLOP CLOCK

The operation of the J-K type flip-flop is to transfer the information present at the J and K inputs just prior to and during the clock pulse to the master flip-flop when the threshold is passed on the leading (positive going voltage) edge of the clock pulse. The information stored in the master flip-flop is transfered to the slave flip-flop, and consequentially to the outputs, when the threshold is passed on the trailing (negative going voltage) edge of the clock pulse. The symbol to indicate this function will be as follows;



J K TYPE FLIP FLOP CLOCK

**D Type Flip-Flop:** The first of these is the D type flip-flop shown in Figure 14 In this element, a single-ended data input (D) is connected directly to the set gate input. An inverter is provided between the input line (D) and the reset input. This ensures that the set and reset levels cannot be high at the same time.




LOGIC SYMBOL

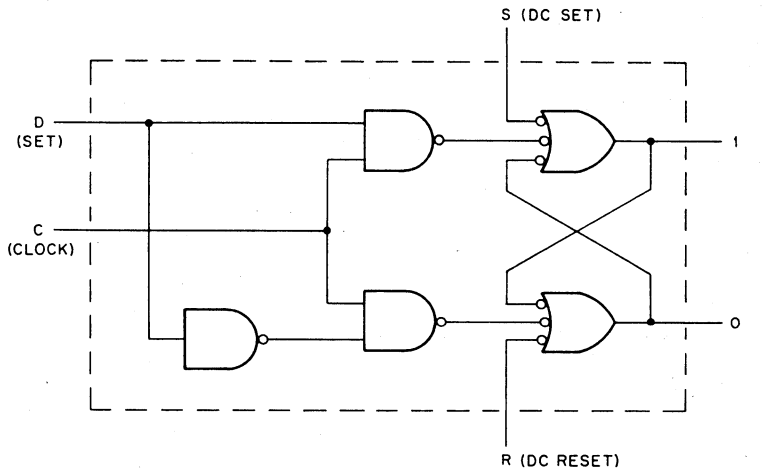



Figure 14. D Type General Purpose Flip-Flop

The flip-flop proper employs three-input NAND gates to provide for dc set and reset inputs.

D type flip-flops are especially suited to buffer register, shift register and binary ripple counter applications. Note that D type devices trigger on the leading (or positive going) edge of the clock pulse. Once the clock has passed threshold, changes on the D input will not affect the state of the flip-flop due to a lockout circuit (not shown).

A characteristic of the D type flip-flop which is not illustrated in the NAND gate equivalent circuit is the fact that the D input is locked out after the clock input threshold voltage on the leading (positive going voltage) edge of the clock has been passed. The D input is not unlocked until the clock input threshold voltage of the trailing (negative going voltage) edge has been passed.

**"MASTER-SLAVE J-K FLIP-FLOP"**

The two unique features of a J-K flip-flop are: A) a clock pulse will not cause any transition in the flip-flop if neither the J nor the K inputs are enabled during the clock pulse, and B) if both the J and the K inputs are enabled during the clock pulse, the flip-flop will complement (change states). There is no indeterminate condition in the operation of a J-K flip-flop.

A word of caution is in order concerning the clock input. The J and K inputs must not be allowed to change states when the clock line is high, the output will complement on the negative going voltage transition of the clock. It is for this reason that the clock line must be kept low until it is desired to transfer information into the flip-flop and no change in the states of the J and K inputs should be allowed when the clock line is high.

The J-K flip-flops used are master-slave devices which transfer information to the outputs on the trailing (negative going voltage) edge of the clock pulse. The J-K flip-flop consists of two flip-flop circuits, a master flip-flop and a slave flip-flop. The information which is present at the J and K inputs when the leading edge threshold is passed and during the clock high will be passed to the master flip-flop (The J and K inputs must not change after the leading edge threshold has been passed). At the end of the clock pulse when the threshold of the clock is passed during the trailing (negative going voltage) edge, the information present in the master flip-flop is passed to the slave flip-flop. If the J input is enabled and the K input is disabled prior to and during the clock pulse, the flip-flop will go to the "1" condition when the trailing edge of the clock occurs. If the K input is enabled and the J input is disabled prior to and during the clock pulse, the flip-flop will go to the "0" condition when the trailing edge of the clock pulse occurs. If both the J and K inputs are enabled prior to and during the clock pulse, the flip-flop will complement when the trailing edge of the clock pulse occurs. If both the J and K inputs are disabled prior to and during the clock pulse, the flip-flop will remain in whatever condition existed prior to the clock pulse when the trailing edge of the clock pulse occurs.

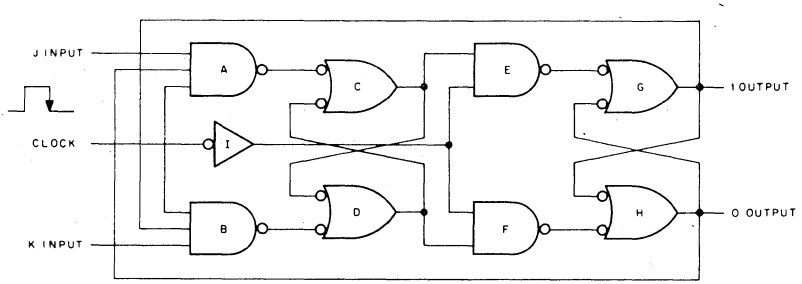



Figure 15. Master-Slave J-K Flip-Flop

Figure 16 shows a functional block diagram of a master slave J-K flip-flop using NAND gates. Gates C and D are the master flip-flop. Gates G and H are the slave flip-flop. Gates A and B are the steering network of the master flip-flop and the steering network for the slave flip-flop is comprised of gates E, F, and 1. The 1 output of the master flip-flop is point X. The operation of the flip-flop will be studied by examining the "1" to "0" transition of the flip-flops, with both the J and the K inputs enabled with a HI level before the clock pulse. When the leading edge of a HI clock pulse occurs, gate B will be enabled with three HI inputs. This will provide a RESET signal for the master flip-flop which will then go to the "0" condition. The slave flip-flop remains in the "1" condition while the clock pulse is HI because gate I is providing a LO signal to both gates E and F, thereby blocking inputs to the slave flip-flop. When the trailing edge of the clock pulse occurs, gate F will be enabled with a HI level at both its inputs and a RESET signal will be provided to the slave flip-flop, which will then go to the "0" condition. The next clock pulse, with both the J and K enabled, would cause the master flip-flop to go to the "1" condition on the leading edge of the clock pulse and cause the slave flip-flop to go to the "1" condition on the trailing edge of the pulse. Figure 16 is a truth table for the J-K flip-flop showing all eight possible initial conditions.

| INITIAL CONDITIONS OUTPUTS | | INPUTS | | FINAL CONDITIONS OUTPUTS | |
|---|---|---|---|---|---|
| 1 | 0 | J | K | 1 | 0 |
| LO | HI | LO | LO | LO | HI |
| LO | HI | LO | HI | LO | HI |
| LO | HI | HI | LO | HI | LO |
| LO | HI | HI | HI | HI | LO |
| HI | LO | LO | LO | HI | LO |
| HI | LO | LO | HI | LO | HI |
| HI | LO | HI | LO | HI | LO |
| HI | LO | HI | HI | LO | HI |

Figure 16. Master-Slave J-K Flip-Flop Truth Table

## UNUSED INPUTS (GATES AND FLIP-FLOPS)

Since the input of a TTL device is an emitter of a multiple-emitter transistor, care must be exercised when an input is not to be used for logic signals. These emitters provide excellent coupling into the driving portions of the circuit when left unconnected. To insure maximum noise immunity, it is necessary to connect these inputs to a source of Logic 1 (High). Two methods are recommended to accomplish this:

1. Connect these inputs to a well filtered and regulated source of +3 volts. Pins U1 and V1 are provided on the M113, M117, M119, M121, M617, and M627 for this purpose.

2. Connect these inputs to one of the active inputs on the same gate. This results in a higher leakage current due to the parallel emitters and should be considered as an additional unit load when calculating the loading of the driving gate.

Connection of unused inputs to the supply voltage, Vcc, is not advisable, since power supplies are subject to transients and voltage excursions which could damage the input transistor.

## TIMING CONSIDERATIONS

**Standard Timing Pulse:** In digital system design, a reference for system timing is usually required. The M Series modules M401 or M405 produces a standard pulse which provides such a reference. The standard pulse derived from each of these two modules is shown in Figure 17.

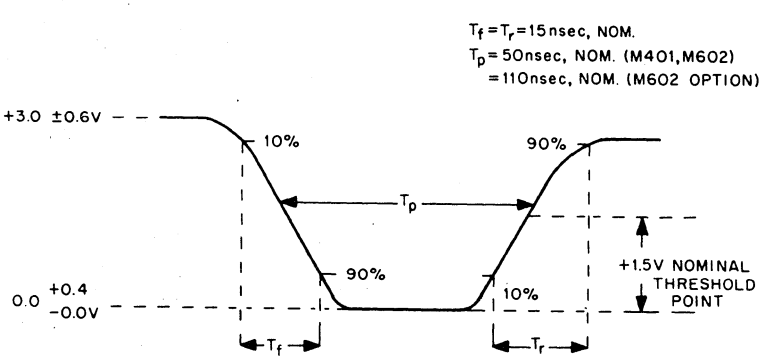


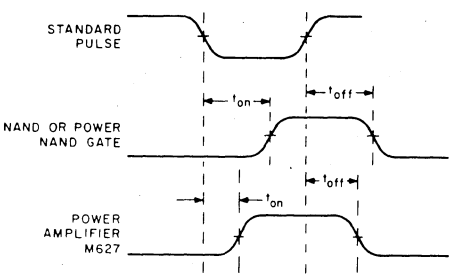

Figure 17. Standard Pulse

**NAND Gate and Power Amplifier Propagation Delays:** The standard pulse (Figure 17) is distributed throughout a system in negative form to maintain the leading edge integrity. (Since the TTL gate drives current in the logic 0 state, the falling edge is more predictable for timing purposes.) However, the standard pulse is of the wrong polarity for use as a clocking input to the type D and J-K flip-flops, requiring the use of a local inverter. Ordinarily, a NAND inverter is adequate. Where high fan-out is necessary, a M617 Power NAND is preferred.

For applications requiring both high fan-out and critical timing the M627 Power Amplifier is available. This module contains extremely high-speed gates which exhibit turn-on times differing by only a few nanoseconds.

Simultaneity is desirable in clock or shift pulses distributed to extended shift registers or synchronous counters.

Delays introduced by inverting gates and power amplifiers are illustrated in Figure 18. (Delays are measured between threshold points.)




| DELAY (NANOSECONDS) | | | |
|---|---|---|---|
| $t_{on}$ | | $t_{off}$ | |
| TYP | MAX | TYP | MAX |
| 18 | 29 | 8 | 15 |
| 7 | — | 5 | — |

Figure 18. NAND Gate and Power Amplifier Delays

**Flip-Flop Propagation Delays:** D type flip-flops trigger on the leading or rising edge of a positive clock pulse; the propagation delay is measured from the threshold point of this edge. The set-up time of the D flop is also measured from this threshold point. Data on the D input must be settled at least 20 nanoseconds prior to the clock transition. The advantage of the D-flip-flop, however, is that the leading edge triggering allows the flip-flop AND gates to propagate while the clock pulse is still high. Figure 19 illustrates this situation.

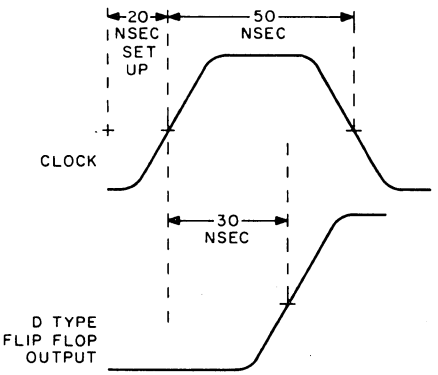



Figure 19. D Type Flip-Flop Timing

JK type flip-flops are, in effect, trailing edge triggering devices as explained previously. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Timing is shown in Figure 20.

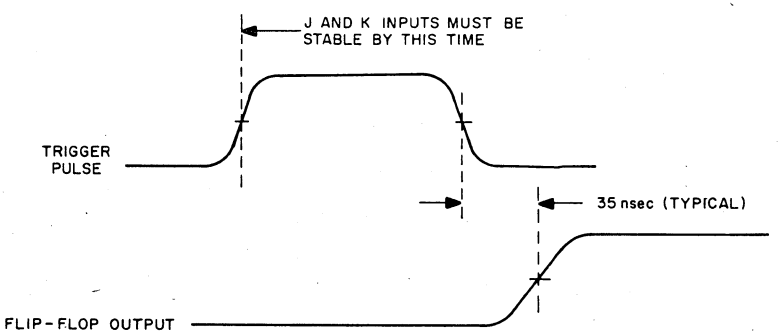



Figure 20. J-K Flip-Flop Timing

When using the dc Set or Reset inputs of either flip-flop type, propagation delays are referenced to the falling edge of the pulse. This is due to the inverted sense of these inputs. When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage) the reset pulse must be longer than the maximum propagation delay of a single stage. This will ensure that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

**One-Shot Delay:** Calibrated time delays of adjustable duration are generated by the M302 Delay Multivibrator. When triggered by a level change from a logical one to a logical zero, this module produces a positive output pulse that is adjustable in duration from 50 to 750 nsec with no added capacitance. Delays up to 7.5 milliseconds are possible without external capacitance. (See M302 specification.) Basic timing and the logic symbol are shown in Figure 21. The 100 picofarad internal capacitance produces a recovery time of 30 nsec. Recovery time with additional capacitance can be calculated using the formula;

$$t_r \text{ Nanoseconds} = 30 \frac{\text{C Total (Picofarads)}}{100}$$

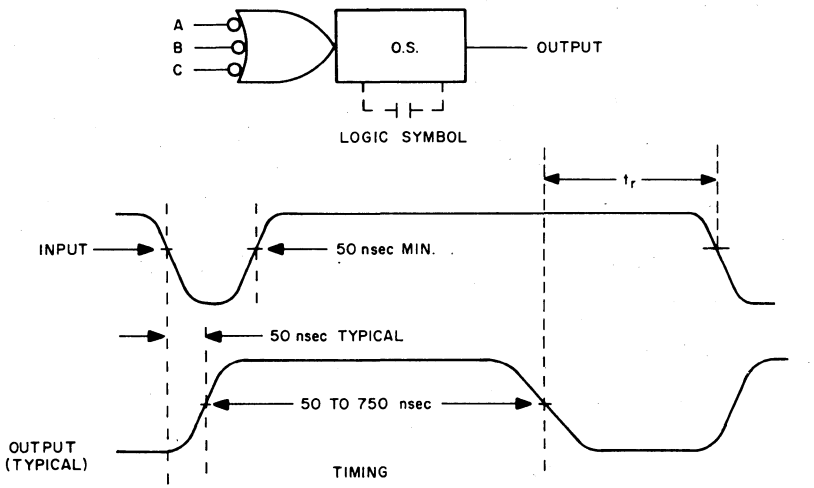



Figure 21. One-Shot Delay Timing and Logic Symbol

**SYSTEM OPERATING FREQUENCY**

Although individual propagation delays are significant in the design of digital logic, even more important is the maximum operating frequency of a system which is composed of these individual modules. Specifically designed systems may be operated at 10 MHz, but a more conservative design may result in a somewhat lower operating speed. M Series modules can be designed into a system with a 6 MHz clock rate with relative ease. This system frequency is derived by summing the delays in a simple logic chain:

1. A standard clock pulse width of 50 nsec is assumed. This period is measured from the threshold point of the leading edge to the threshold point of the trailing edge.

2. One flip-flop propagation delay of 35 nsec from the trailing edge of the clock pulse to the threshold point of the final state of the flip-flop is allowed.

3. Two gate-pair delays of 30 nsec each are assumed. (A gate-pair consists of two inverting gates in series.) Two gate-pair delays are usually required to perform a significant logic function with a minimum of parallel operations. The two gate-pair delays total 60 nsec.

The time necessary to perform these operations before the next occurrence of the clock pulse is the sum of the delays; 50 + 35 + 60, or 145 nsec. Allowing 20 nsec for variations within the system, the resulting period is 165 nsec, corresponding to a 6 MHz clock rate. This timing is demonstrated in Figure 22.

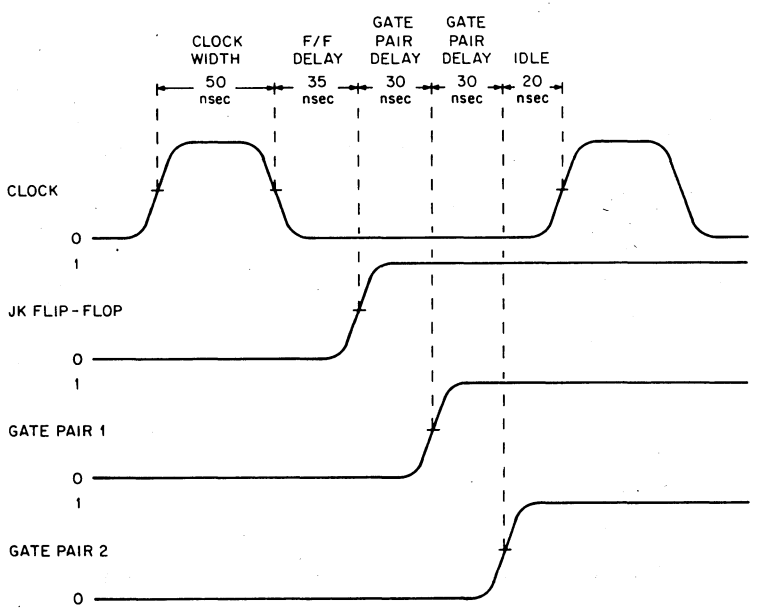
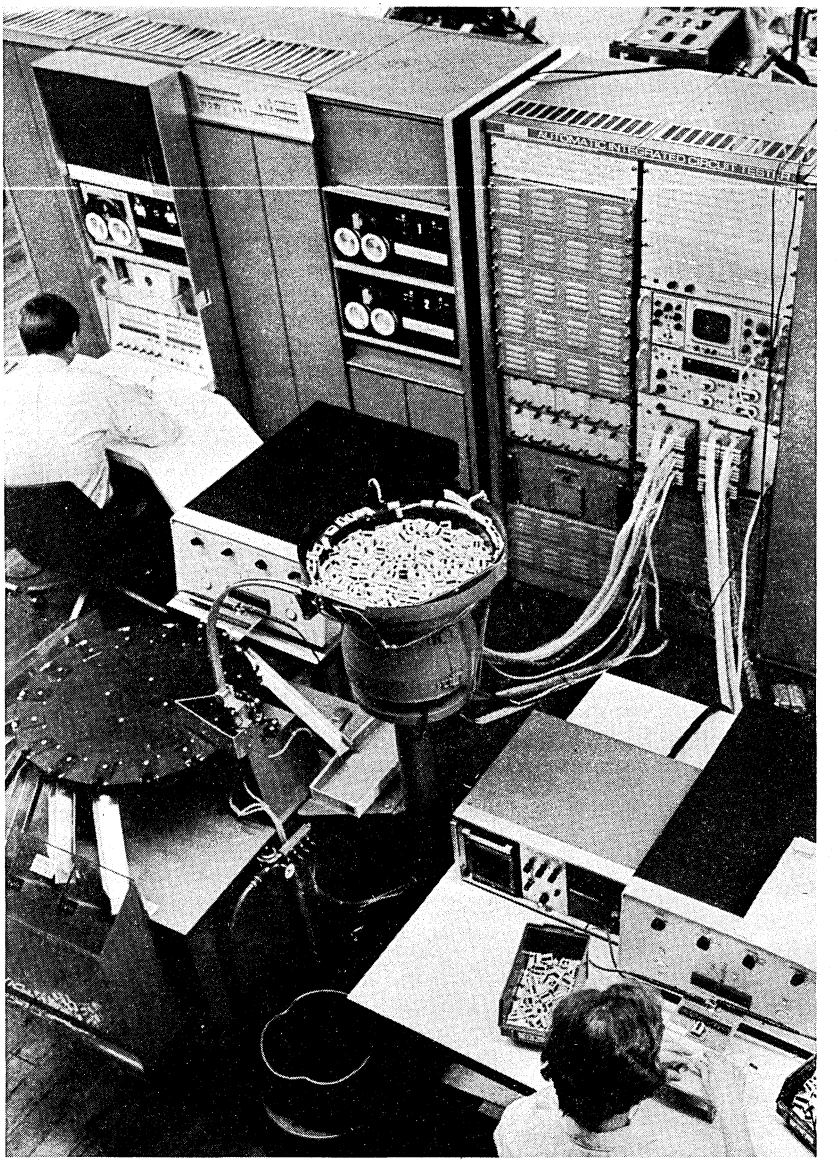



Figure 22. Delays Determining System Operating Frequency

Substitution of a D type flip-flop results in a similar timing situation. In a system using both D and J-K flip-flops, note that the D flip-flop triggers on the leading edge of the clock pulse and the J-K flip-flop triggers on the trailing edge. When calculating system timing using D flip-flops, remember that the flip-flop inputs must be settled at least 20 nsec prior to the occurrence of the clock pulse.

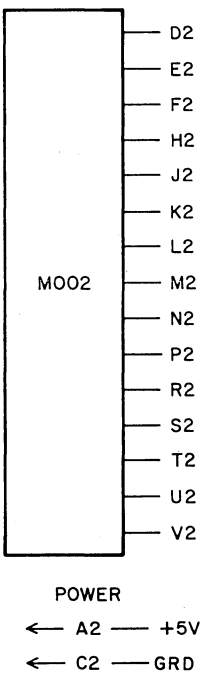
Preparation of a timing diagram that considers delays introduced by all logic elements will aid the designer in achieving predictable system performance.



All incoming integrated circuits undergo computer controlled testing, with 40 dc and 16 ac tests performed in 1.1 seconds. This 100% inspection speeds production by minimizing the diagnosis of component failures in module test.

# LOGIC 1 SOURCE
M002

**M SERIES**



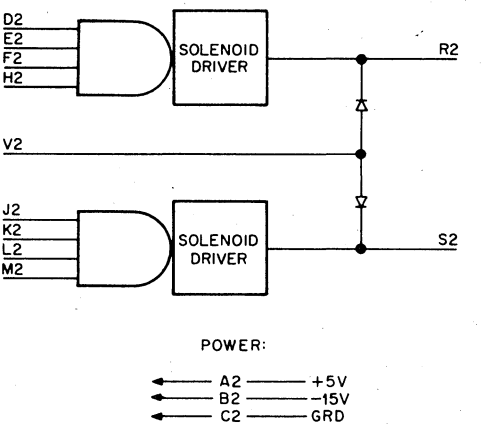

To hold unused M-Series TTL gate inputs high, the M002 provides 15 outputs at +3 volts (Logic 1), on pins D2 through V2. Up to 10 unused M-Series gate inputs may be connected to any one output. If a M002 circuit is driven by a gate, it appears as two TTL unit loads or 3.2 ma. at ground.

**Power:** +5 v at 16 ma. (max.)

M002 — $10

# SOLENOID DRIVER
## M040

**M SERIES**




M040 Solenoid Driver

These high current drivers can drive relays, solenoids, stepping motor windings, or other similar loads. The output levels are —2 volts and a more negative voltage determined by an external power supply. One terminal of the load device should be connected to the external power source, the other to the driver output. There are two drivers per module.

Pin V of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than 3 feet long it may have to be by-passed at the module with an electrolytic capacitor to reduce the short over-shoot caused by the inductance of the wire. If pin V is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.

**Inputs:** Each input presents one unit load.

**Outputs:** The M040 has maximum ratings of —70 volts and 0.6 amp. Typical delay for the circuit is 5 μsec. No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits.

**Grounding:** High current loads should be grounded at pin C2 of the M040. —15 volt at 9 ma. (max.)

**Power:** +5 volt at 47 ma. (max.)

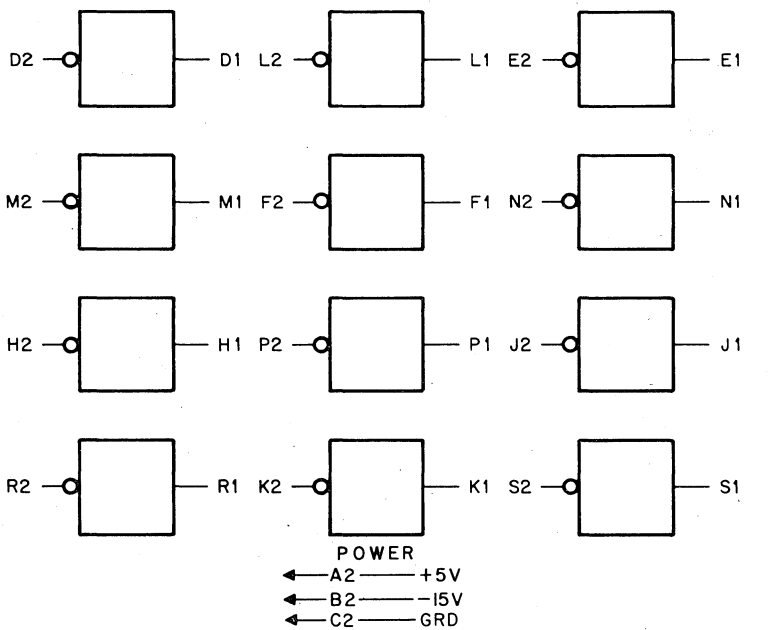
The external voltage supply must provide the output current of the two drivers. (1.2 amps. max.)

Note:
Refer to K Series driver modules for increased current drive, increased voltage breakdown or AC current drive capability.

M040 — $39

# 50 MA. INDICATOR DRIVER
M050

**M SERIES**




**M050 INDICATOR DRIVER**

The M050 contains twelve transistor inverters that can drive miniature incandescent bulbs such as those on an indicator panel. It is used to provide drive current for a remote indicator, such as Drake 11-504, Dialco 39-28-375, or Digital Indicator type 4908, or level conversion to drive 4917 and 4918 indicator boards (See the Hardware Section.) A low level on the input of the driver causes current to flow in the output.

**Inputs:** Each input presents two unit loads.

**Outputs:** Each output is capable of driving 50 ma. into an external load connected to any voltage between ground and −30 volts.

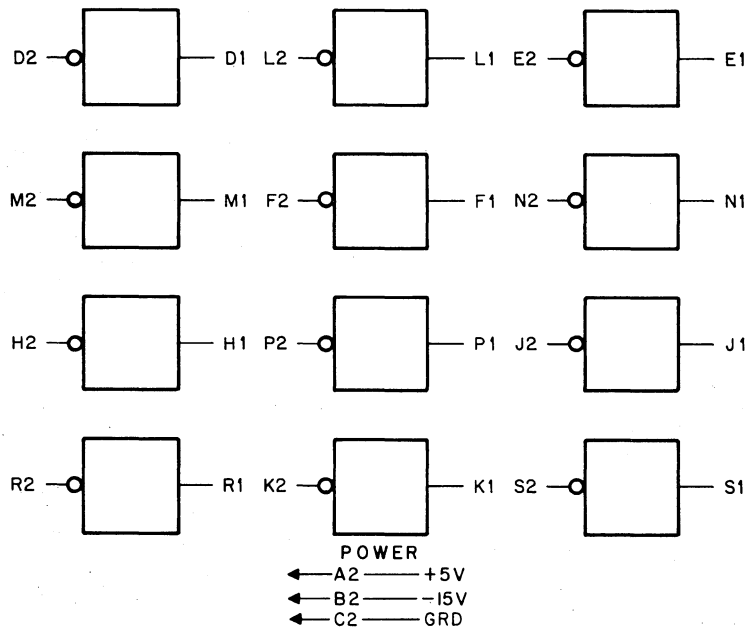
**Power:** +5 volt at 47 ma. (max.)
−15 volt at 16 ma. (max.)

**Note:** For those applications requiring the sinking of current, refer to K Series.

M050—$31

# LEVEL CONVERTER
M051

**M SERIES**




The M051 contains twelve level converters that can be used to shift M and K Series logic levels to negative logic levels of ground and —3 volts. A grounded input on the driver generates a grounded output.

**Inputs:** Each input presents two TTL unit loads.

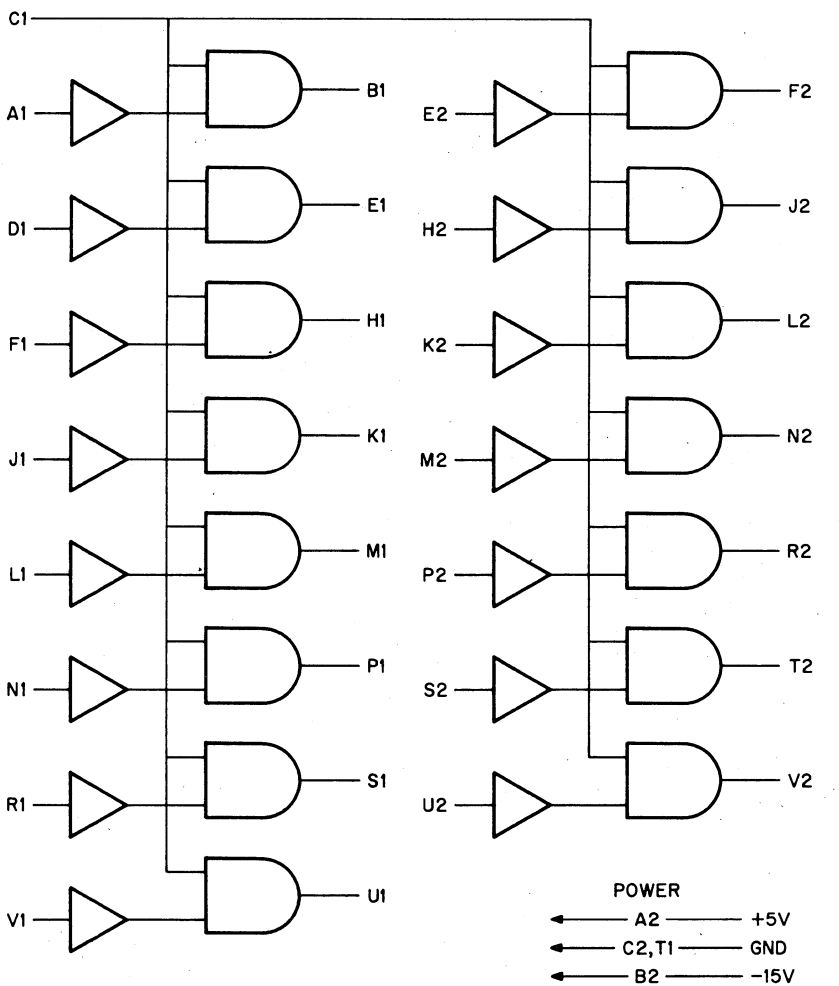
**Outputs:** The output consists of an open collector PNP transistor and can drive 20 ma. to ground —6V maximum may be applied to the output.

**Power:** +5V at 47 ma. (max.); —15V at 16 ma. (max.)

M051—$31

# BUS DATA INTERFACE
## M100

**M SERIES**




The M100 Bus Data Interface contains fifteen circuits for convenient reception of data from the PDP-8, PDP-8/I negative voltage bus. It is pin compatible with the M101 Positive Bus Data Interface.

The loading presented to the negative voltage bus differs from that loading using the standard negative bus modules (i.e., R107, R111) in that the data lines are loaded only if the appropriate device is selected. The option select output of the M102 must be connected to the strobe input pin, C1, of the M100.

The enabling line of the M100 cannot be used as a strobe line. The output signals are indeterminant for a period of 200 nsec after the enabling line has become true.

**Inputs:** All outputs will drive 10 TTL unit loads.

**Conversion:** Logic Diagram: An active voltage is a True State, i.e., −3 v **or** +3v = "1".
A ground is a $\overline{\text{True}}$ State.
A data input of −3v will yield an output of ground when C1 is gated by a positive voltage logic "1" of +2.4 volts.

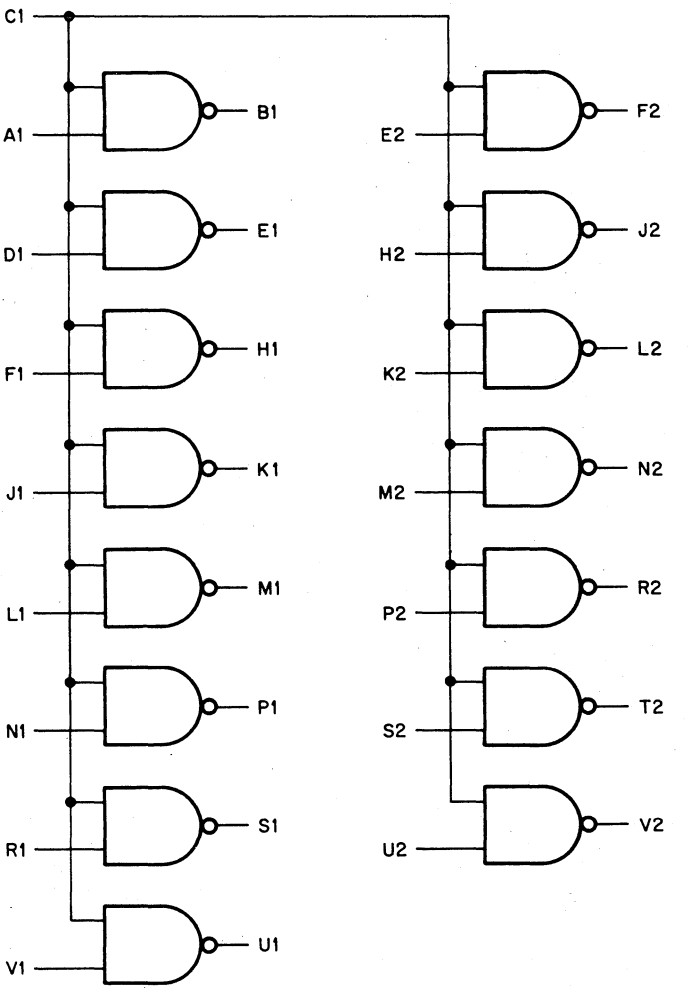
**Threshold switching level:** −1.5 v. typ.

**Propagation delay:** 40 nsec typ.

**Power:** +5 volts at 60 ma. (max.); −15 volts at 10 ma. (max.)

# BUS DATA INTERFACE
M101

**M SERIES**




POWER

← A2 — +5V

← C2, T1 — GRD

The M101 contains fifteen, two-input NAND gates arranged for convenient data strobing off of the PDP8/I or PDP8/L positive bus. One input of each gate is tied to a common line so that all data signals on the second input of each gate can be enabled simultaneously. The M101 can also be used as inverters or a data multiplexer. All data inputs are protected from a negative of more than —0.8 volts.

**Inputs:** Each data signal input presents one TTL unit load. The common line input presents fifteen unit loads.

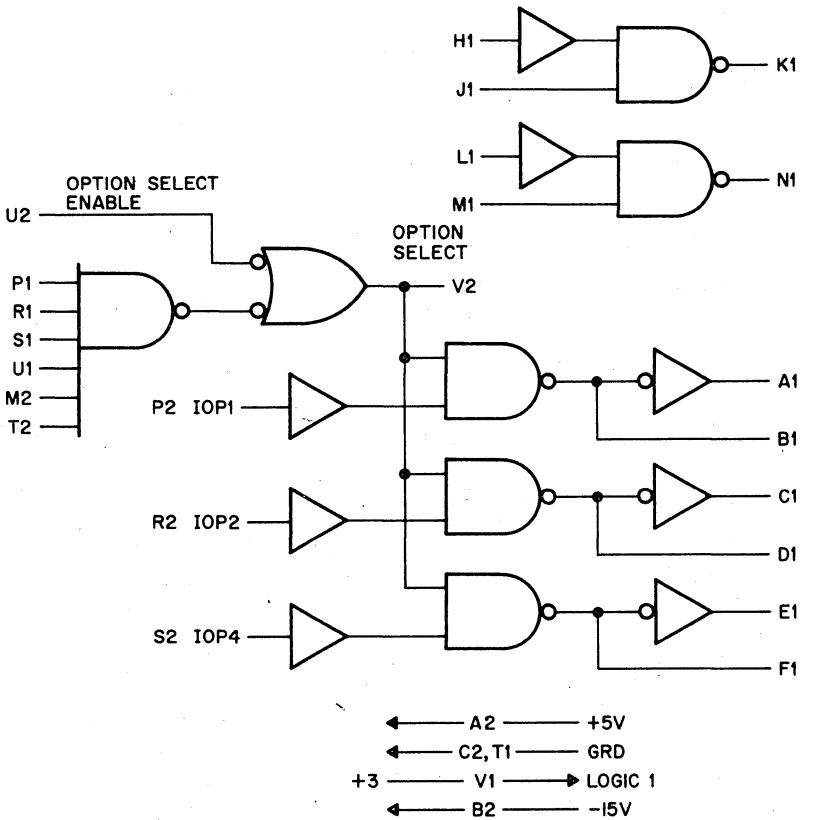
**Outputs:** Each output can drive ten unit loads.

**Power:** +5V at 82 ma. (max.)

M101—$24

# DEVICE SELECTOR
## M102

**M SERIES**




The M102 is used to decode the six device address bits transmitted in complementary pairs on the negative bus of the PDP-8, PDP-8/I. The outputs of the M102 are compatible with M Series TTL logic. The M102 is pin compatible with the M103 Positive bus device selector with the exception of the address inputs. The true state of the BMB outputs of the PDP-8 and PDP-8/I are defined as ground where the true states of the PDP-8/I positive bus and PDP-8/L are defined as an active voltage state. This fact requires that the complement of the address bits used for an M103 must be connected to the M102.

As the address complement is tied to the pins D2, E2, F2, H2, J2, K2, an M103 may be directly substituted for an M102 when changing from a negative to a positive bus.

**Inputs:** U2 represents 1.25 TTL unit loads, J1, M1 represents 1 TTL, P1, R1, S1, U1, M2 and T2 standard levels of −3 volt and ground. Input load is 1 ma. shared among the inputs that are at ground.

P2, R2, S2, H1 and L1
0.2 ma. when V in = 0v
0.0 ma. when V in = −3v
Propagation Delay 40 nsec typ.

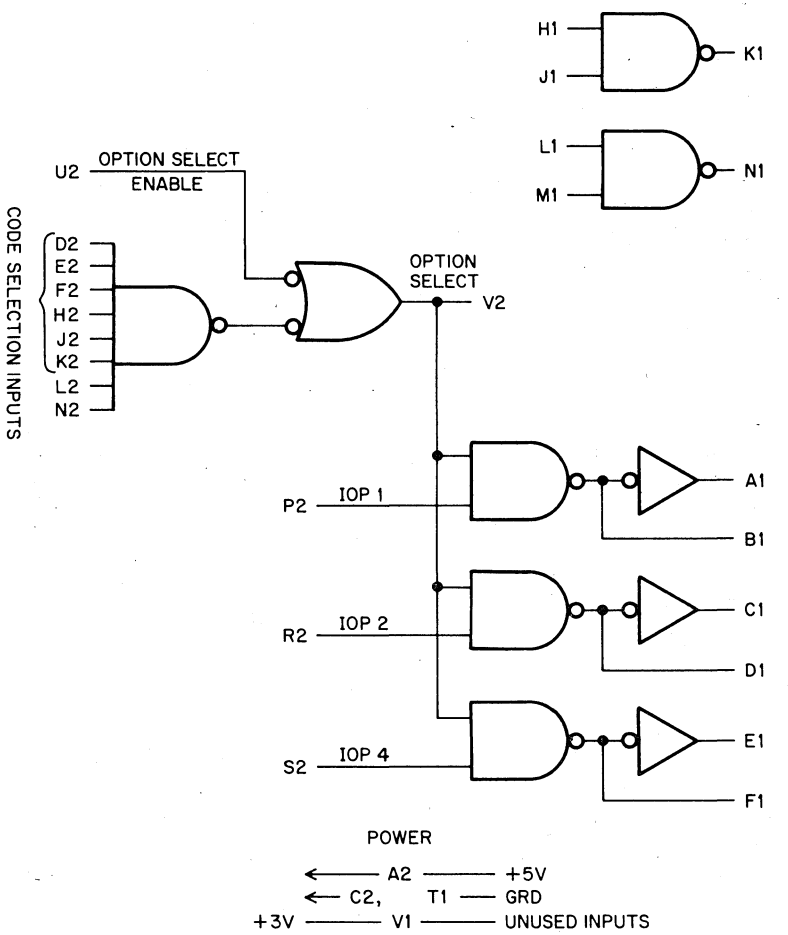
**Outputs:** K1 and M1 can drive 10 TTL unit loads. A1, B1, C1, D1, E1, F1 can each drive 37 TTL unit loads. U2 can drive 16 TTL unit loads.

**Conversion:** Logic Diagram. An active voltage is a True State, i.e., −3v or +3v = "1". A ground is a True State.

**Power:** +5 volts at 130 ma. (max.); −15 volts at 40 ma. (max.)

# DEVICE SELECTOR
M103

**M SERIES**




The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP8/I and PDP8/L. Selection codes are obtained by selective wiring of the bus signals to the code select inputs D2, E2, F2, H2, J2, and K2. This module also includes pulse buffering gates for the IOP signals found on the positive bus of the above computers. Two two-input NAND gates are also provided for any additional buffering that is required.

**Inputs:** All inputs which receive positive bus signals are protected from negative voltage undershoot of more than —0.8V.

The following inputs each present one TTL unit load D2, E2, F2, H2, J2, K2 H1, J1, L1, and M1. Inputs P2, R2, and S2 present 2.5 TTL unit loads. Inputs U2, L2 and N2 each present 1.25 unit loads. These inputs need not be tied to a source of logic 1 when not used.

**Outputs:** Gate outputs K1 and N1 can each drive ten TTL unit loads.

Pulse buffering outputs A1, B1, C1, D1, E1 and F1 can each drive 37 TTL unit loads.

The Option Select output can drive 16 TTL unit loads.

**Power:** +5 volts at 110 ma. (max.)

# DEVICE SELECTOR
## M107

**M SERIES**

The M107 is a device selector which, by the use of extended decoding of the BMB lines 9 through 11, will provide seven discrete IOT pulses. Five additional IOT pulse outputs are provided to allow the user to reduce software requirements by the combining of IOT codes. The IOT instruction and the IOP times at which the various IOT pulses occur at the module pins are outlined in the following chart:

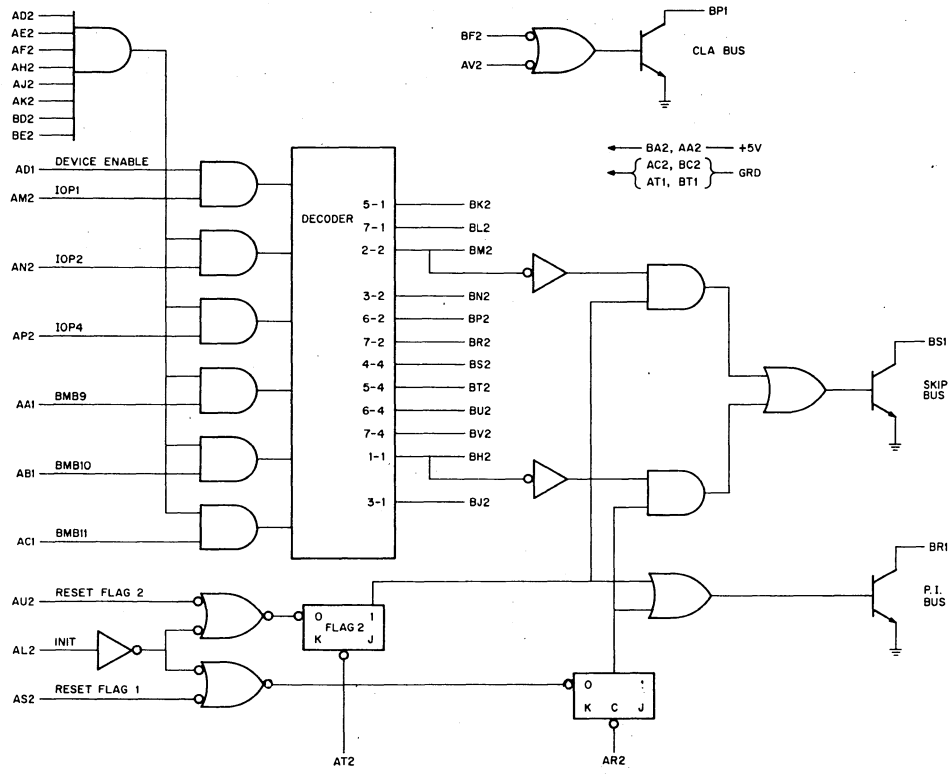
| Module Pin | IOT | AT IOP TIME | | |
|---|---|---|---|---|
| | | 1 | 2 | 4 |
| BH2 | 1 – 1 | X | | |
| BM2 | 2 – 2 | | X | |
| BJ2 | 3 – 1 | X | | |
| BN2 | 3 – 2 | | X | |
| BS2 | 4 – 4 | | | X |
| BK2 | 5 – 1 | X | | |
| BT2 | 5 – 4 | | | X |
| BP2 | 6 – 2 | | X | |
| BU2 | 6 – 4 | | | X |
| BL2 | 7 – 1 | X | | |
| BR2 | 7 – 2 | | X | |
| BV2 | 7 – 4 | | | X |

Example: If an IOP-7 is issued, IOT pulses will exist only at output pins BL2 (7-1), BR2 (7-2) and BV2 (7-4). IOT pulses will not exist at any other output pin.

The M107 also contains two flag flip-flops which may be directly cleared or set. The outputs of the flag flip-flops are connected to the skip and program interrupt lines. Interrogation of the flags is accomplished by IOT 1 – 1 for flag 1 and IOT 2 – 2 for flag 2.

The M107 also provides two inputs to accomplish the "clear the accumulator" function.

**INPUTS:** Pins — AD2, AE2, AF2, AH2,
AJ2, AK2, AA1, AB1,
AC1, AL2, AV2, BF2,
Present one TTL load


AD2
AE2
AF2
AH2
AJ2
AK2
BD2
BE2
DEVICE ENABLE
AD1
IOP1
AM2
IOP2
AN2
IOP4
AP2
BMB9
AA1
BMB10
AB1
BMB11
AC1
DECODER
5-1
7-1
2-2
3-2
6-2
7-2
4-4
5-4
6-4
7-4
1-1
3-1
BK2
BL2
BM2
BN2
BP2
BR2
BS2
BT2
BU2
BV2
BH2
BJ2
BF2
AV2
BP1
CLA BUS
BA2, AA2
+5V
AC2, BC2
AT1, BT1
GRD
BS1
SKIP BUS
BR1
P.I. BUS
AU2
RESET FLAG 2
AL2
INIT
AS2
RESET FLAG 1
FLAG 2
K
J
AT2
K
C
J
AR2

**INPUTS:** Pins — BD2, BE2, AM2, AN2,
AP2, AU2, AS2
Present 1.25 TTL load.

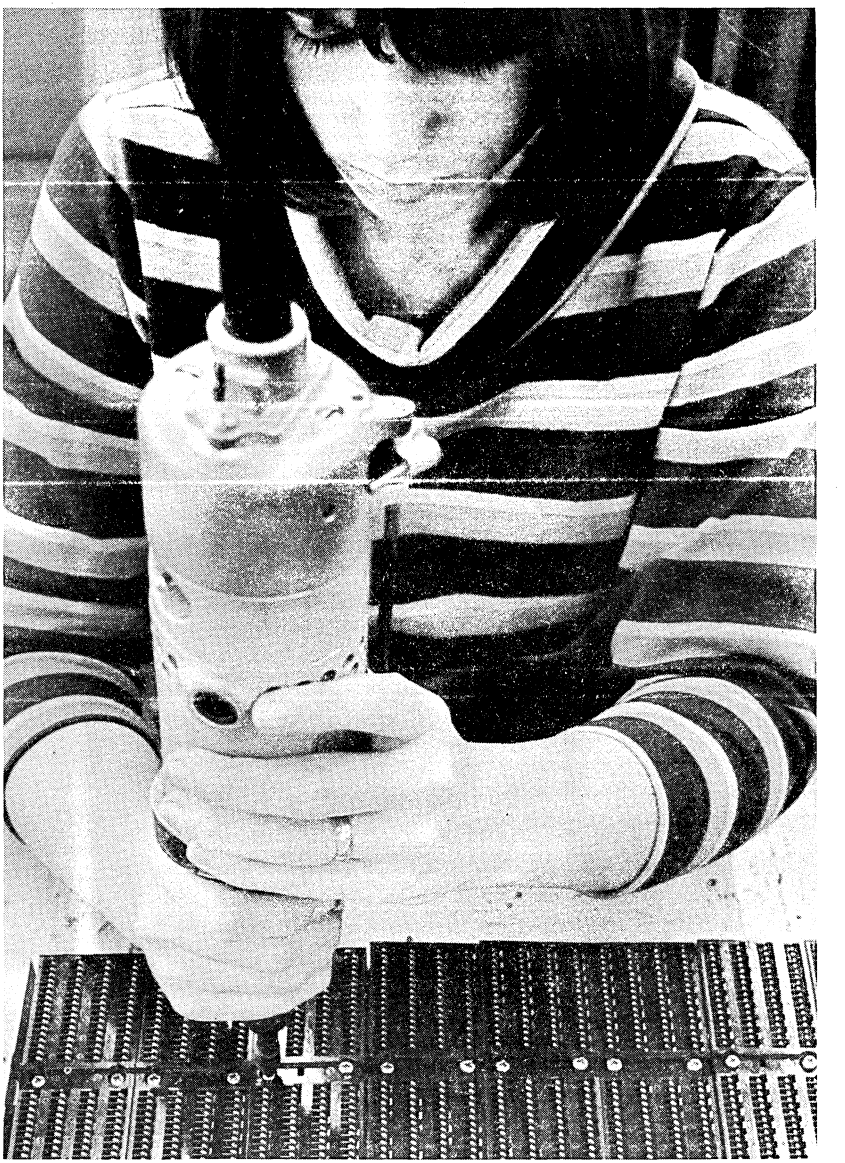
Pins — AR2, AT2 resent 2 TTL loads.

**Outputs:** Option Select Pin AD1 can drive 13 TTL loads. Bus driver outputs pins BP1, BS1, and BR1 are open collector NPN transistors and can sink 30 ma. at ground. The maximum voltage applied to these outputs must not exceed +20 volts and each output is diode protected against negative undershoot in excess of −0.9 volts.

All other outputs will drive up to 35 TTL loads.

**Power:** +5v at 245 ma. (maximum).

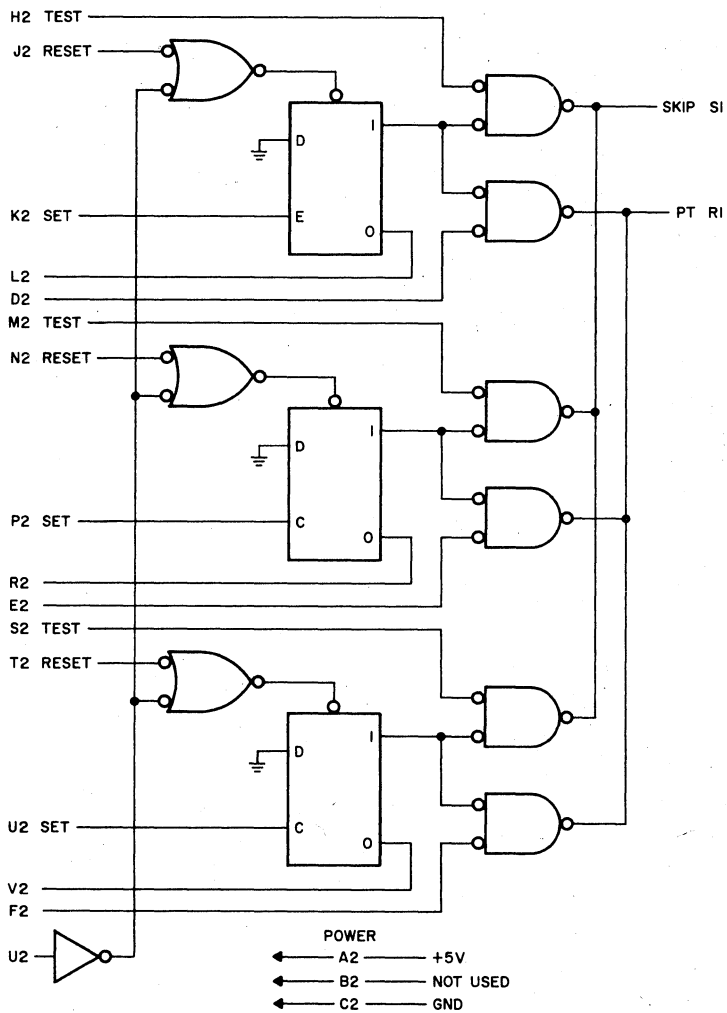
M107 — $105



Far more is done on The Module Assembly floor than the name implies. Subassemblies as well as module testing, are produced to keep pace with DEC's growth.

# FLAG MODULE
M108

M
SERIES



The M108 is a single height module and contains three flag flip-flops. Each flag flip-flop may be independently cleared or all flip-flops may be cleared simultaneously.

The output of each flag flip-flop is gateable and are open collector "OR"ed to the Program Interrupt bus.

The output of each flag flip-flop is passed through a gate and open collector to the skip bus. This facility allows the user to test for a flag.

The "0" side of each flip-flop has been extended to module pins for peripheral control.

Each flip-flop may be independently set by the application of the leading (positive going voltage) edge of a pulse or level to the clock inputs.

If it is not desired to disable the Program Interrupt gate, internal circuitry is provided which makes it unnecessary to connect these inputs to a source of logic "1".

**Inputs:** K2, P2, U2, present 2 TTL loads. D2, E2, F2 present 1.25 TTL loads. All other inputs present 1 TTL load.

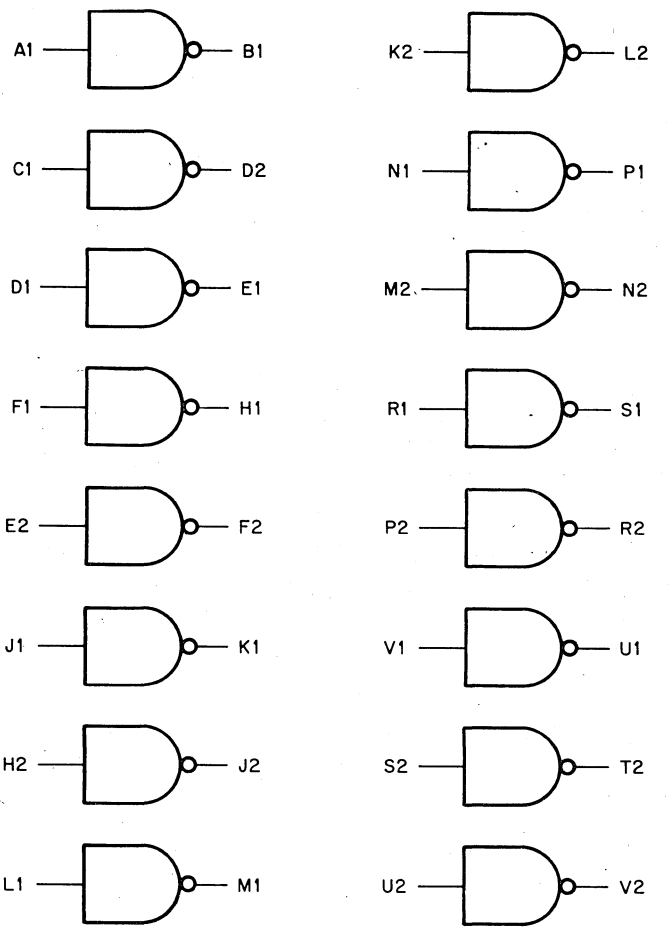
**Outputs:** L2, R2, V2 supply 9 TTL loads. R1 (P. I. Function) and S1 (Skip Function) are open collector NPN Transistors and will sink 100mA to ground. The voltage applied to these outputs must not exceed +20 volts.

**Power:** +5 volts at 137 ma. (max.)

M108 — $45

# INVERTER
M111

**M SERIES**




POWER

← A2 —— +5V

← C2, T1 —— GRD

Sixteen Inverters with input/output connections as shown.

**Input:** Each input presents one unit load.

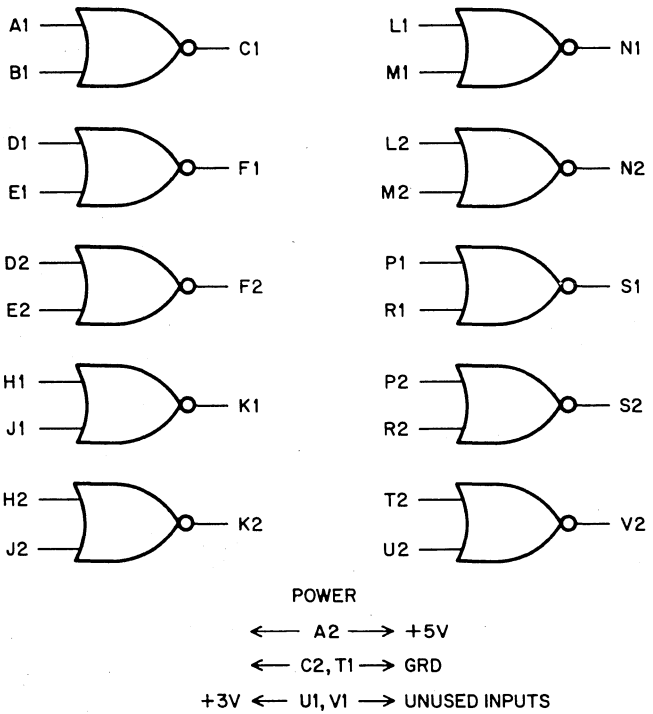
**Output:** Each output can drive up to ten unit loads.

**Power:** +5 volts, 87 ma. (max.)

M111 — $22

# NOR GATE
M112

**M SERIES**




The M112 contains ten positive NOR gates, each performing the function A + B. Pins U1 and V1 provide +3 volts, each capable of holding High (Logic 1) up to 40 unused M-Series inputs.

**Input:** Each input presents one unit load.

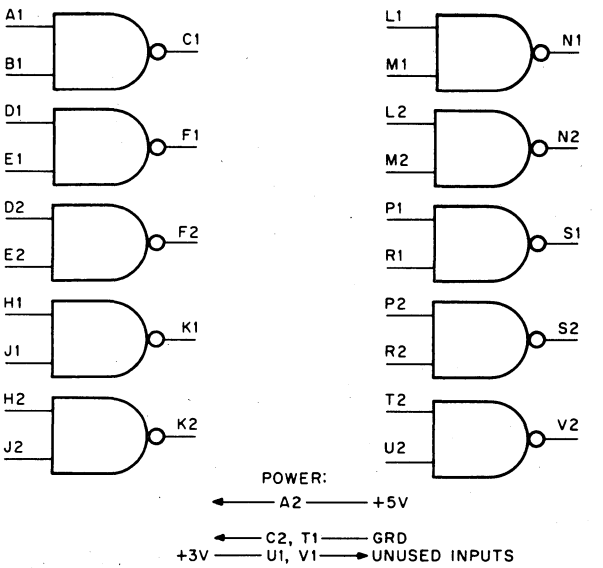
**Output:** Each output can drive up to ten unit loads.

**Power:** +5V at 50 ma. (max.)

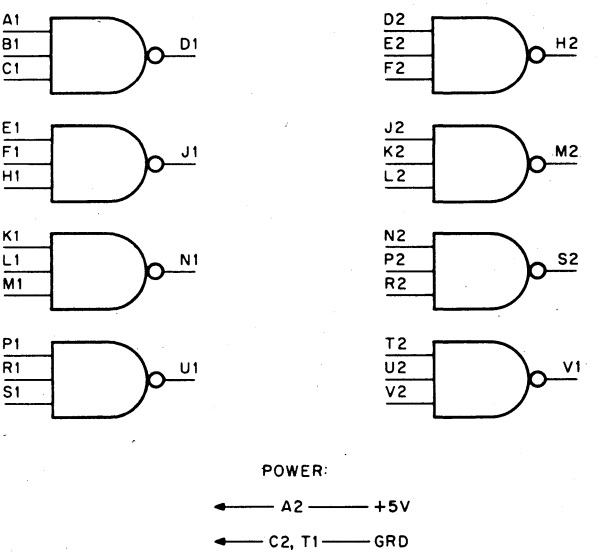
M112 — $35

# NAND GATES
## M113, M115, M117, M119

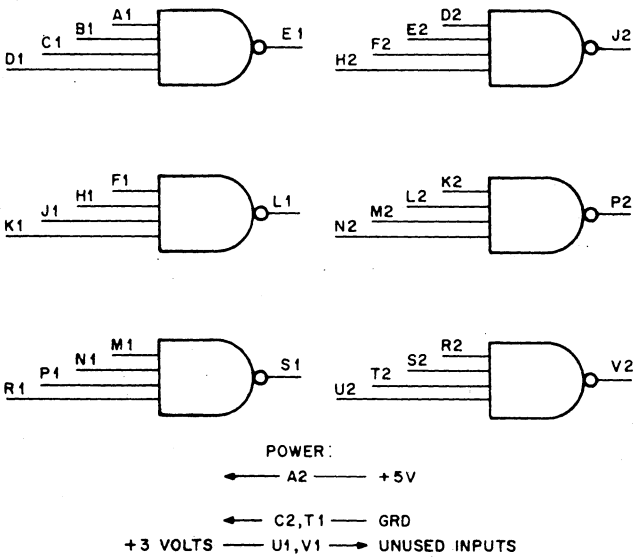
**M SERIES**



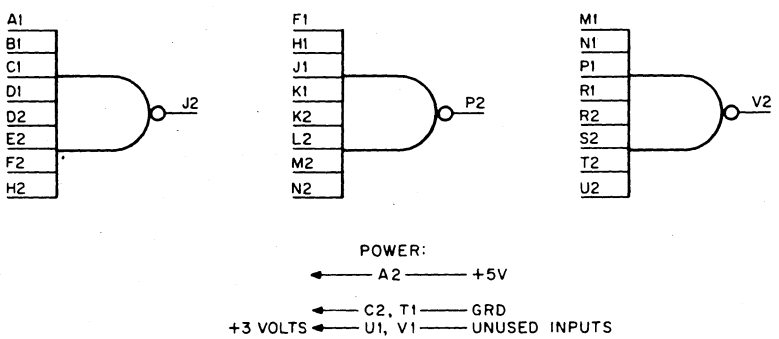

M113 2-INPUT NAND GATES




M115 3-INPUT NAND GATES




M117 4-INPUT NAND GATES




M119 8-INPUT NAND GATES

These modules provide general-purpose gating for the M Series, and are most commonly used for decoding, comparison, and control. Each module performs the NAND function A • B - - - - - - - - - N, depending upon the number of inputs.

M113—Ten, two-input NAND gates that also may be used as inverters.

M115—Eight, three-input NAND gates.
M117—Six, four-input NAND gates.
M119—Three, eight-input NAND gates.

Unused inputs on any gate must be returned to a source of logic 1, for maximum noise immunity. In the M113, M117, M119, M121, M617 and M627 modules, two pins are provided (U1 and V1) as source of +3 volts for this purpose. Each pin can supply up to 40 unit loads.

M103, M111 and M002 provide additional sources of logic 1 level.

Typical propagation delay of M Series gates is 15 nsec.

**Inputs:** Each input presents one unit load.

**Outputs:** Each output is capable of supplying 10 unit loads.

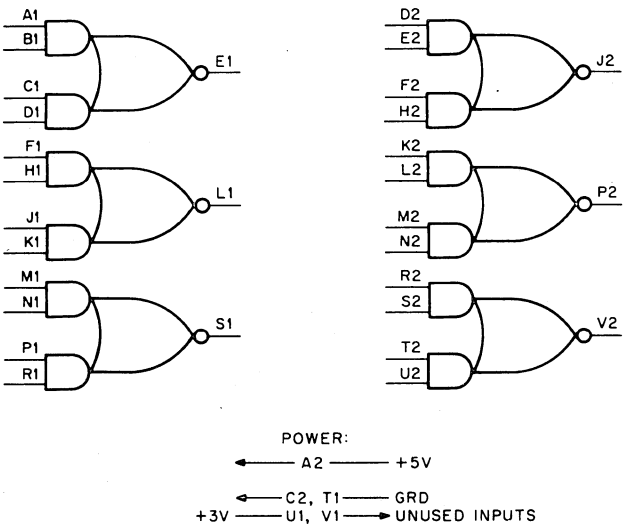
**Power:**

| | | |
|---|---|---|
| M113: | 71 ma. | } +Max. current at 5 volts. |
| M115: | 41 ma. | |
| M117: | 41 ma. | |
| M119: | 19 ma. | |

| |
|---|
| M113 — $18 |
| M115 — $18 |
| M117 — $19 |
| M119 — $18 |

# AND/NOR GATE
M121

**M SERIES**




M121 AND/NOR GATES

The M121 module contains six AND/NOR gates which perform the function AB + CD. By proper connection of signals to the AND inputs, the exclusive OR, coincidence, and NOR functions can be performed.

Typical propagation delay of an M121 gate is 15 nsec.

**Inputs:** Each input presents one unit load to the driving module.

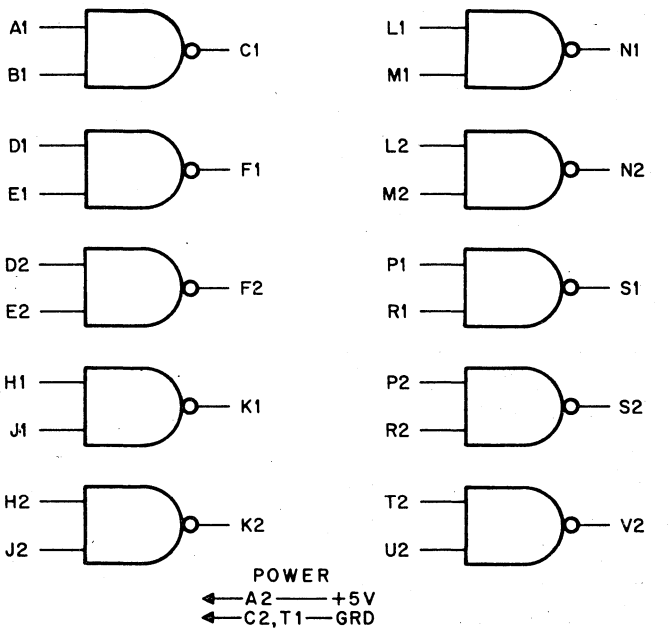
**Outputs:** Each output is capable of driving up to 10 unit loads.

**Power:** +5volt at 50 ma. (max.)

M121 — $23

# INPUT NAND GATES
M133

**M SERIES**




This module provides general purpose high speed gating for the M-Series. Maximum output propagation delay to a logic 1 or 0 is 10 nsec. The high speed characteristic of these gates frequently will solve tight timing problems in complex systems. Unused inputs on any gate must be returned to a source of logic 1 for maximum speed and noise immunity.

**Inputs:** Each input presents 1.25 unit loads.

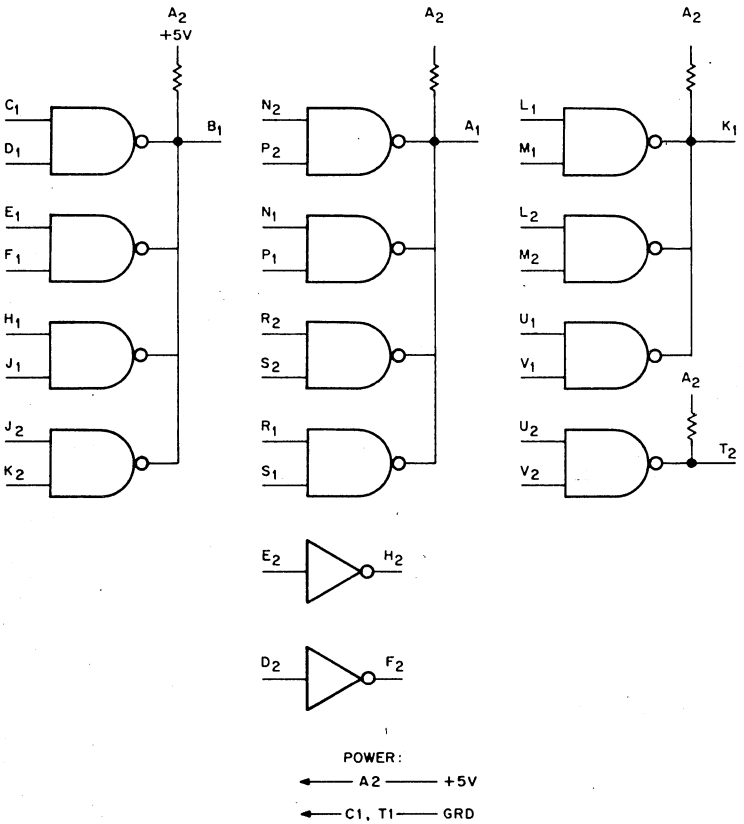
**Outputs:** Each output is capable of driving 12.5 unit loads.

**Power:** +5V at 160 ma. (max.)

M133 — $27

# NAND/OR GATES
## M141

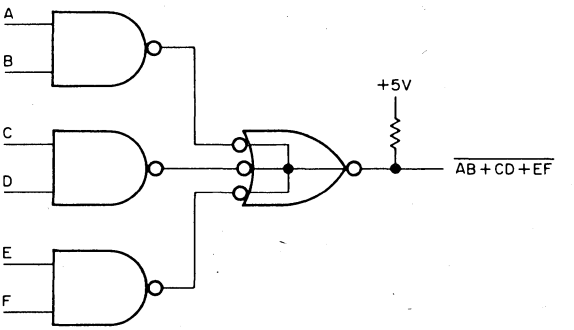
**M SERIES**




M141 NAND/OR GATE

The M141 NAND/OR gate performs two levels of logic. The first is the NAND function which is identical to the M113 NAND gate. The second level is that of a wired OR for low logic levels. The two input NAND gate which is used in the M141 does not have the standard TTL output circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor. Propagation delay through these gates is a maximum of 70 nsec.

The NAND/OR gates are arranged in four groups consisting of 4, 4, 3, and 1 two input NAND gates respectively. The outputs in each group are connected together which provide a wired OR for low levels. The function of these gates can be shown as:




By using one of the two inverters provided, a true AND/OR function can be realized. A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together.

**Inputs:** Each input presents one unit load.

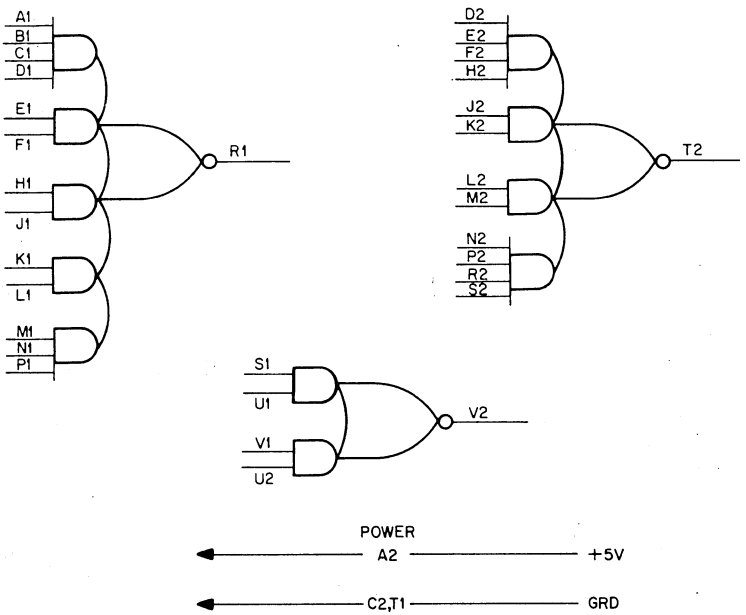
**Outputs:** Four gate outputs, each capable of driving 7 unit loads. The load resistor of each output presents 2 unit loads when connected to another output. For example, four groups are connected together, therefore 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability. Each inverter output is capable of driving up to 10 unit loads.

**Power:** +5 volts at 117 ma. (max.)

M141 — $29

# AND/NOR GATE
M160

M SERIES




M160 AND/NOR GATES

The M160 module contains three general purpose AND/NOR gates which perform functions similar to the M121. By connecting signals to the AND inputs, these gates can be used to select and place on a single output any of several input signals.

Typical propagation delay of an M160 gate is 20 nsec.

**Inputs:** Each input presents one unit load

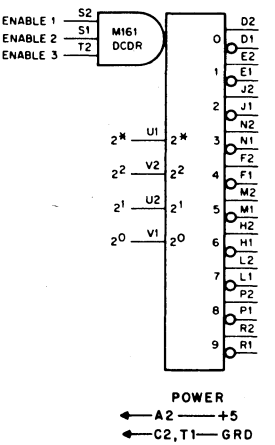
**Outputs:** Each output is capable of driving 10 unit loads

**Power:** 5 volt at 30 ma. (max.)

M160 — $33

# BINARY TO OCTAL/DECIMAL DECODER
## M161

**M SERIES**




M161 BINARY TO OCTAL/DECIMAL DECODER

The M161 is a functional decoding module which can be used as a binary-to-octal or binary-coded decimal (8421 or 2421 codes) to decimal decoder. In the binary-to-octal configuration, up to eight M161's can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2* input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4 modules) are shown below. The figure assumes that the inputs to the decoder are the outputs of flip-flops such as FF2° (1), 1 output side; and FF2° (0), 0 output side.

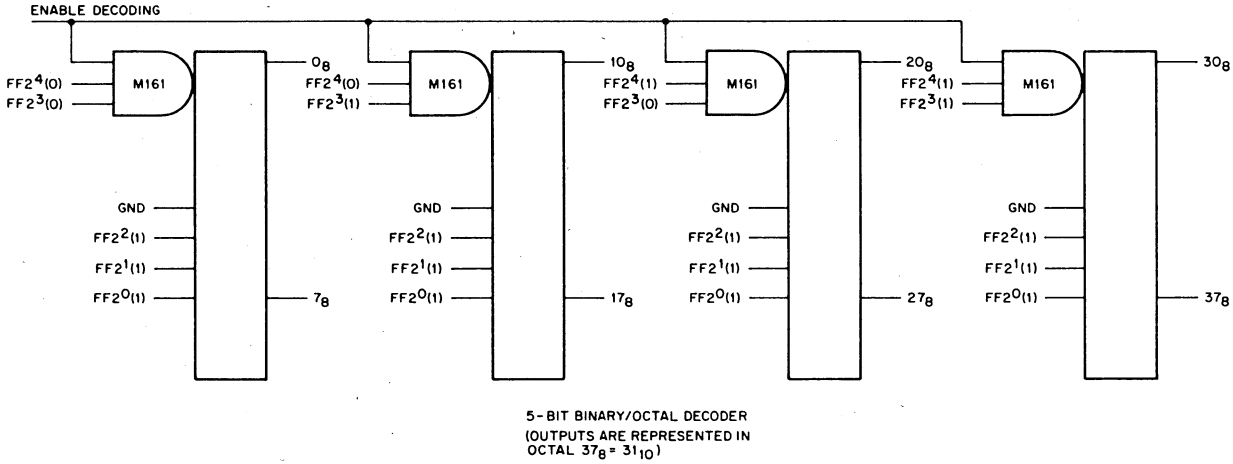
The 2* input may be of decimal value 2, 4, 6, 8 as long as illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.

The propagation delay through the decoder is typically 55 nsec in the binary-to-octal mode, and 75 nsec in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 nsec, frequency-limiting this module to 8HMz when used in this fashion. The enable inputs can be used to strobe output data providing inputs 2° — 2* have settled at least 50 nsec prior to the input pulse.

**Inputs:** 2° through 2*, 1 unit load each; ENABLE 1 through ENABLE 3, 2 unit loads each.

**Outputs:** Each positive output is capable of driving 10 unit loads, and each negative output, 9 unit loads.

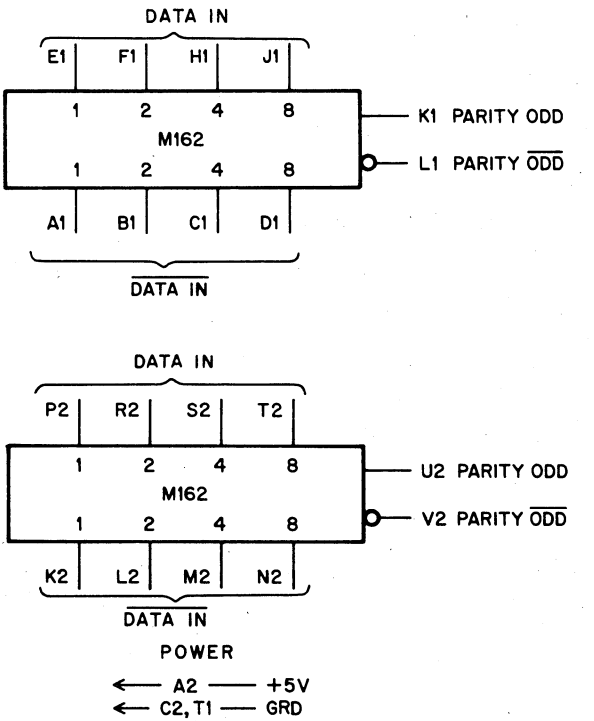
**Power:** 5 volts at 120 ma. (max.)




## 5-BIT BINARY/OCTAL DECODER

# PARITY CIRCUIT
## M162

**M SERIES**




The M162 is a parity detector and contains two Parity Circuits. Each circuit indicates whether the Binary Data presented to it contains an ODD or EVEN number of ONES. The DATA and its complement are required as shown.

Indication of ODD PARITY is given by a High level of pins K1 and U2 respectively. Pins L1 and V2, when High, indicate EVEN PARITY or no input.

**Input:** Each input presents four unit loads.

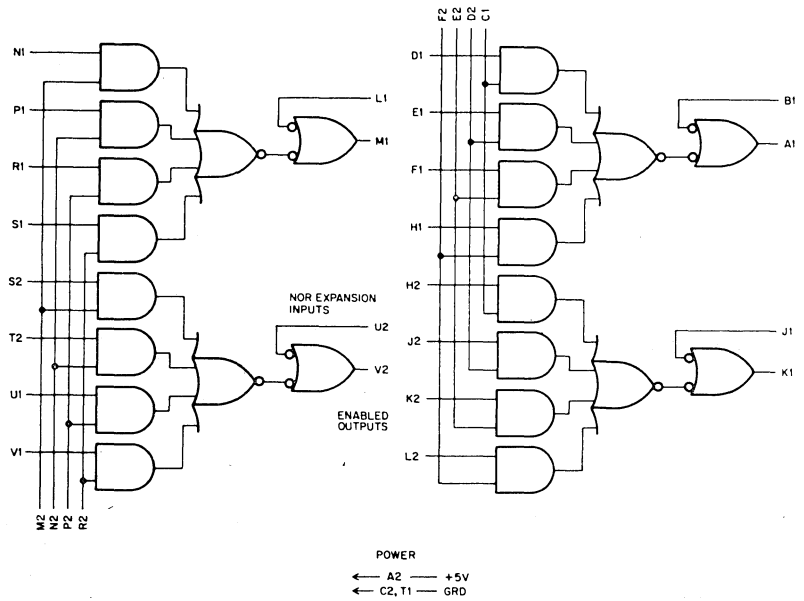
**Output:** Pins L1 and V2 can each supply up to ten unit loads. Pin K1 and U2 can each supply up to six unit loads.

**Power:** +5 volts at 102 ma. (max.)

M162 — $63

# GATING MODULE
## M169

**M SERIES**




M169 GATING MODULE

The M169 provides a general gating function, and may be used as a four-output multiplexer. Raising High a DATA INPUT and selecting a corresponding INPUT ENABLE line, generates a High at the appropriate ENABLED OUTPUT, A1, K1, M1 or V2. Any of the ENABLED OUTPUTS may be enabled directly through an M121 or M160 AND/NOR gate, used as an NOR Expander. Maximum input to output propagation delay for any circuit is 45 nsec.

**Inputs:** Each DATA INPUT pin and EXPANSION INPUT pin presents one unit load. Each INPUT ENABLE pin presents two unit loads.

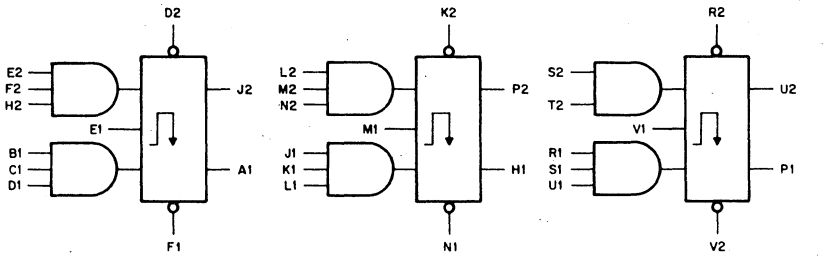
**Outputs:** Each output can drive up to ten unit loads.

**Power:** +5 volts at 50 ma. (max.)

M169 — $33

# TRIPLE J-K FLIP-FLOP
## M202

**M SERIES**




A2, +5V
C2, T1, GROUND
B2, NOT USED

The M202 contains three J-K flip-flops augmented by multiple-input and gates. For general use as gated control flip flops or buffers.

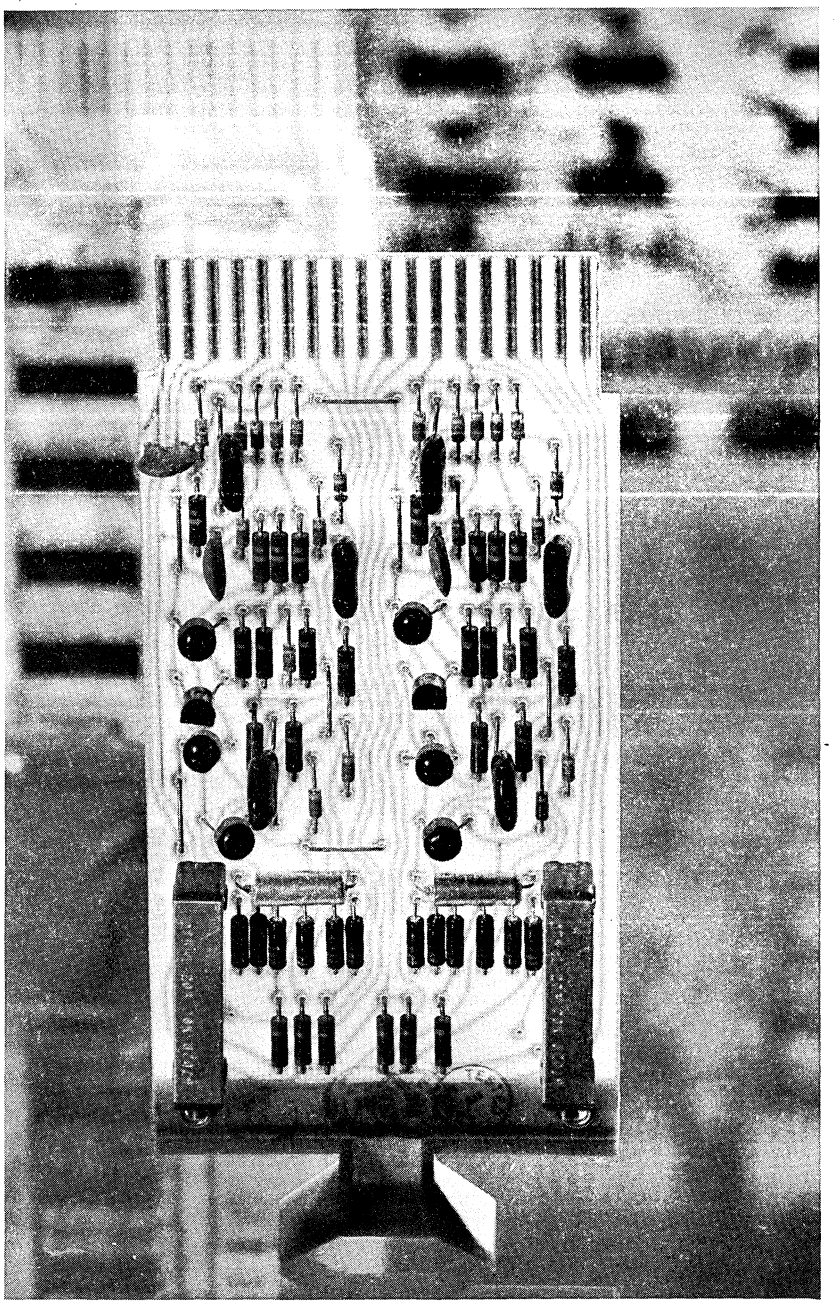
Logical operation of the J-K flip flops used in this module is identical to those flip-flops used in the M207 (described in detail) except clock, J-K inputs, inputs, direct clear, direct set and both output lines for each flip-flop are independent.

**Inputs:** All gate inputs represent 1 unit load. The dc set and clear input each represent two unit loads. Clock inputs represent two unit loads.

**Outputs:** Each output will drive 10 unit loads.

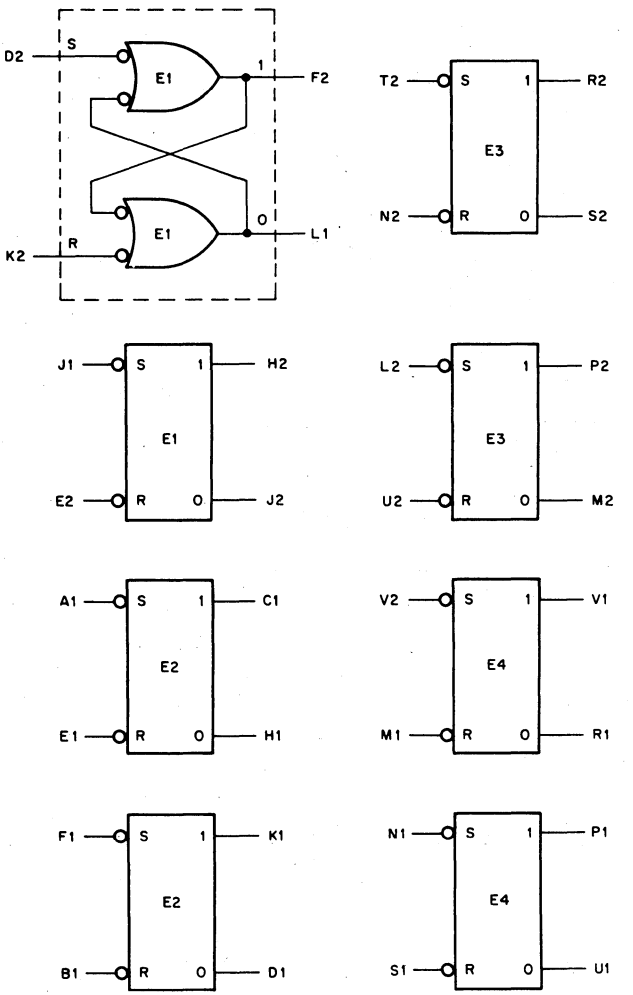
**Power:** +5 v at 57 ma. (max.)

M202 — $29



# 8-R/S FLIP-FLOPS
## M203

**M SERIES**




M203 8-R/S FLIP-FLOPS

The M203 is made up of 8 R/S type flip-flops. Each flip-flop is made up of two 2-input NAND gates whose outputs are cross coupled. R/S flip-flops provide an inexpensive method of storage but care must be taken to inhibit placing the Set and Reset inputs low at the same time. In this case, the last of the inputs to be removed will control the final state of the flip-flop.

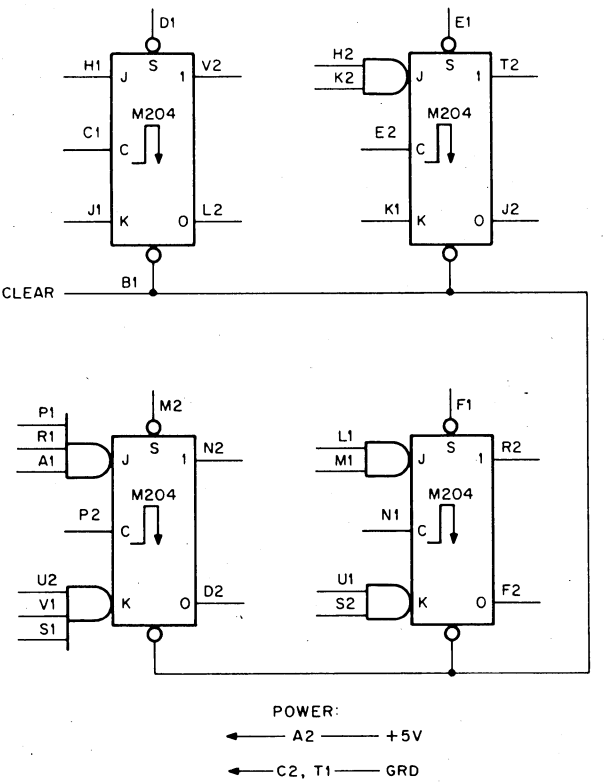
The propagation delay of the M203 is approximately 30 nsec.

**Inputs:** All inputs present 1 unit load.

**Outputs:** All outputs are capable of driving 9 unit loads.

**Power:** +5 volts, 55 ma. (max.)

M203 — $26




M204 GENERAL-PURPOSE BUFFER AND COUNTER

The M204 contains four J-K type flip-flops, augmented by multiple-input AND gates, for general use as gated control flip-flops or buffers. The gating scheme permits the formation of counters of most moduli up to 16, by simple connector wiring. Clock, trigger and input lines for each flip-flop are independent. A common CLEAR input is provided.

Input information is transferred to the outputs when the threshold point is reached on the trailing (negative going voltage) edge of the clock pulse.

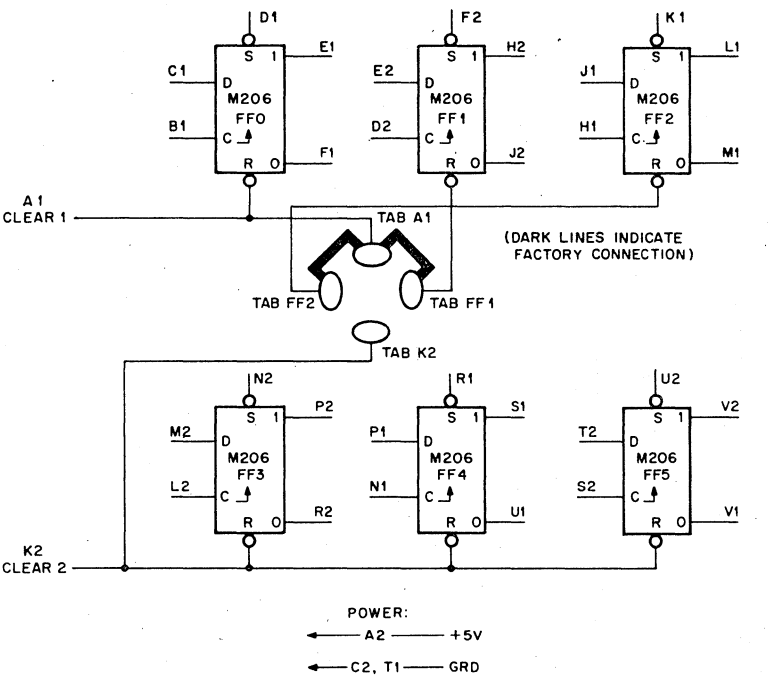
Logical operation of the J-K flip-flops used in this module is identical to the M207 (described in detail) except for the addition of dc set inputs.

**Inputs:** The "C" inputs present two unit loads each to the source. The dc set ("S") inputs present two unit loads each. The common CLEAR line presents 8 unit loads. All other inputs present one unit load to the source.

**Outputs:** Each output, before interconnection as a counter, is capable of driving 10 unit loads.

**Power:** +5 volts, 74 ma. (max.)

M204 — $34




## M206 D TYPE FLIP-FLOPS

The M206 contains six separate D-Type flip-flops. Each flip-flop has independent gated data, clock, and dc set inputs.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

| CONFIGURATION | CLEAR 1 (A1) | CLEAR 2 (K2) | DELETE JUMPER | ADD JUMPER |
|---|---|---|---|---|
| 3-3 | FF0, 1, & 2 | FF3, 4, & 5 | | |
| 4-2 | FF0 & 1 | FF2, 3, 4, & 5 | A1 to FF2 | K2 to FF2 |
| 5-1 | FF0 | FF1, 2, 3, 4, & 5 | A1 to FF2<br>A1 to FF1 | K2 to FF2<br>K2 to FF1 |

Information must be present on the D input 20 nsec (max) prior to a standard clock pulse and should remain at the input at least 5 nsec (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 nsec, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

Information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

**Inputs:** D inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 3 unit loads per connected flip-flop. S inputs present 2 unit loads each.

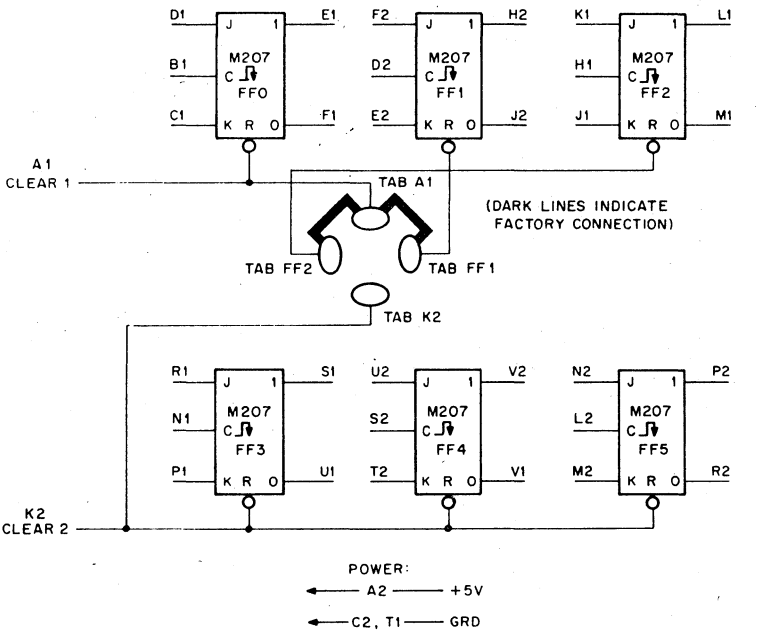
**Outputs:** Each output is capable of driving 10 unit loads.
**Power:** +5 volts, 87 ma. (max.)

A common clear for all six flip-flops can be obtained by wiring pins A1 and K2 together externally. **CAUTION:** The loading of each clear line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

M206 — $30

# GENERAL-PURPOSE FLIP-FLOP
M207

**M SERIES**




M207 J-K FLIP FLOPS

The M207 contains six J-K type flip-flops which can be used as buffers, control flip-flops, shift registers, and counters. A truth table for clocked set and reset conditions appears below. Note that when the J and K inputs are both high, the flip-flop complements on each clock pulse.

| STARTING CONDITION (OUTPUT) | | INPUT CONDITION | | RESULT AT END OF STANDARD CLOCK PULSE (OUTPUT) | |
|---|---|---|---|---|---|
| 1 | 0 | J | K | 1 | 0 |
| L | H | L | L | No change | |
| | | L | H | No change | |
| | | H | L | H | L |
| | | H | H | H | L |
| H | L | L | L | No change | |
| | | L | H | L | H |
| | | H | L | No change | |
| | | H | H | L | H |

Application of a low level to an R input for at least 25 nsec resets the flip-flop unconditionally. Two CLEAR inputs are provided, with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0.

J and K inputs must be stable during the leading-edge threshold of a standard clock input and must remain stable during the positive state of the clock. Data transferred into the flip-flop will be stable at the output within 30 nsec (typical) of the clock pulse trailing edge threshold (negative going voltage).

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flop. All M207 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

| CONFIGURATION | CLEAR 1 (A1) | CLEAR 2 (K2) | DELETE JUMPER | ADD JUMPER |
|---|---|---|---|---|
| 3-3 | FF0, 1, & 2 | FF3, 4, & 5 | | |
| 4-2 | FF0 & 1 | FF2, 3, 4, & 5 | A1 to FF2 | K2 to FF2 |
| 5-1 | FF0 | FF1, 2, 3, 4, & 5 | A1 to FF2 | K2 to FF2 |
| | | | A1 to FF1 | K2 to FF1 |

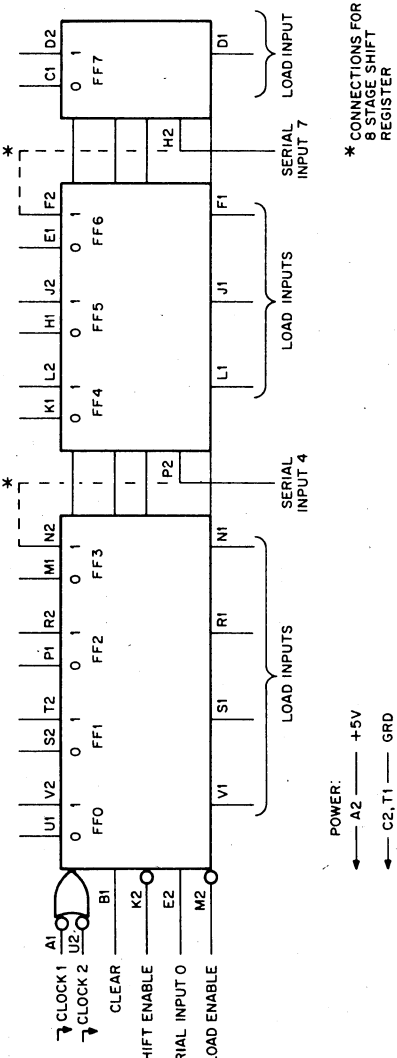
**Inputs:** J or K inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 2 unit loads per connected flip-flop.

**Outputs:** Each output is capable of driving 10 unit loads.

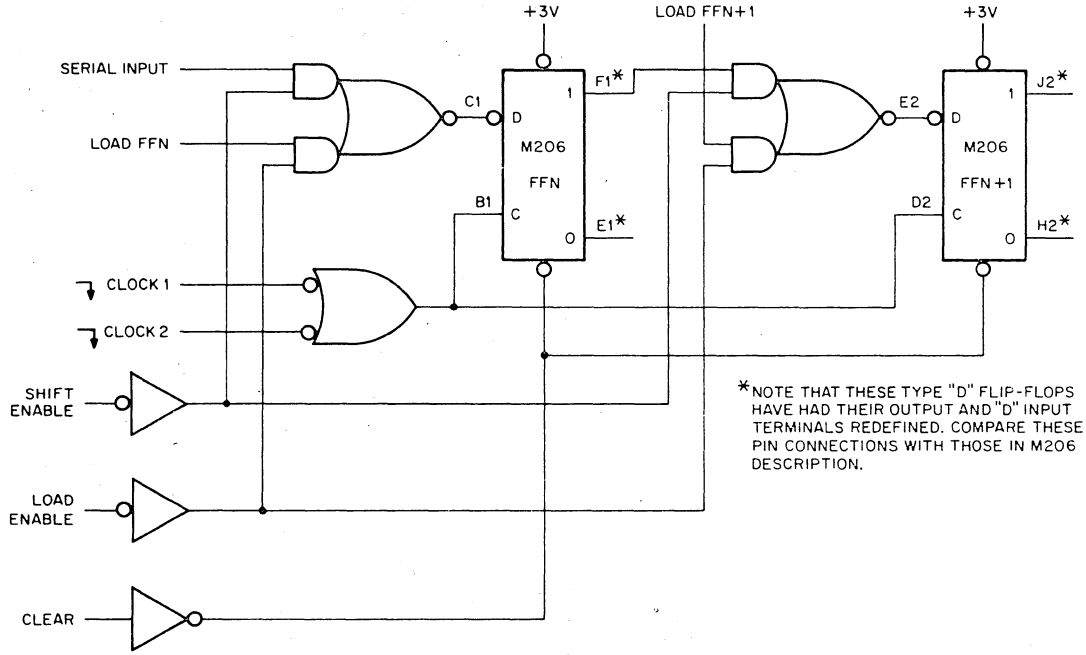
**Power:** +5 volts, 96 ma. (max.)

# 8-BIT BUFFER/SHIFT REGISTER
## M208

**M SERIES**




M208 8-BIT BUFFER/SHIFT REGISTER




TWO REPRESENTATIVE STAGES

The M208 is an internally connected 8-bit buffer/shift register. Provisions are made for gated single-ended parallel load, bipolar parellel output, and serial input. The shift register is divided into three segments:

Bits 0 through 3: Serial input to bit 0, bipolar outputs from bits 0 through 3.

Bits 4 through 6: Serial input to bit 4, bipolar outputs from bits 4 through 6.

Bit 7: Serial input to 7, bipolar outputs from bit 7.

Each of these groups shares a common shift line (the ORed CLOCK 1 and CLOCK 2 inputs) and a common parallel load line (LOAD ENABLE). To form a 6-bit shift register, for example, the true output of bit 3 is connected to the serial input of stage 4. A shift register of 8 bits may be constructed from a single module. Modules may be cascaded to form shift registers of any desired length. A few additional stages may be formed more economically from NAND and AND/NOR gates plus a D-type flip-flop. A representative stage of this type is illustrated.

Two clock inputs are provided so that individual Load and Shift clock sources may be used. Care must be taken that the clock inputs remain in the high state in the off condition because either input going to the low state will produce a positive edge at the output of the NAND gate and trigger the D type flip-flop. Data shifted or parallel loaded into the M208 will appear on the outputs within 55 nsec (max) of the clock pulse leading edge threshold. Load of Shift Enable levels and parallel data must be present at least 50 nsec prior to a clock pulse. Propagation delay from the leading edge of a CLEAR pulse to the outputs is 40 nsec max.

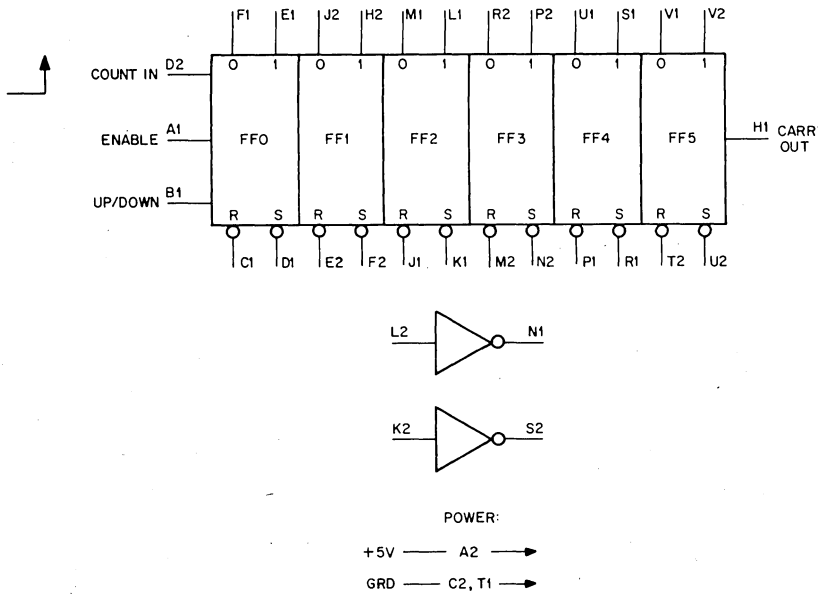
**Inputs:** Serial data, dc set, and enable inputs present one unit load each to the source module. Each clock input presents 2½ unit loads. The CLEAR input presents two unit loads.

**Outputs:** Parallel outputs are capable of driving 10 unit loads each.

**Power:** +5 volts, 184 ma. (max.)

# BINARY UP/DOWN COUNTER
## M211

**M SERIES**




M211 BINARY UP/DOWN COUNTER

The M211 is a 6 bit binary UP/DOWN counter. It can switch counting mode (UP or DOWN) without disturbing the contents of the counter. Maximum count rate is 10 MHz. SET/RESET inputs are available for each bit. Maximum carry propagation time is 80 ns per bit.

**Enable Line:** The Enable input must be negated 100 nsec. prior to an UP/DOWN level command.

The Enable input must **not** be negated earlier than 500 nsec. after the leading edge (positive going voltage) of the clock pulse.

The Enable input must be asserted at least 60 nsec. prior to the first count.

**UP/DOWN Control Line:** A logical 1 on this line will yield an up count.

A logical 0 on this line will yield a down count.

**Carry Out:** The Carry Out will yield a positive level change whenever a carry or borrow occurs.

**Inputs:** Count In—positive transition or pulse with less than 400 nsec rise-time. Count In presents 2 unit loads. Reset—Each reset input presents 3 unit loads. Set—Each set input presents 2 units loads. All other inputs present 1 unit load.

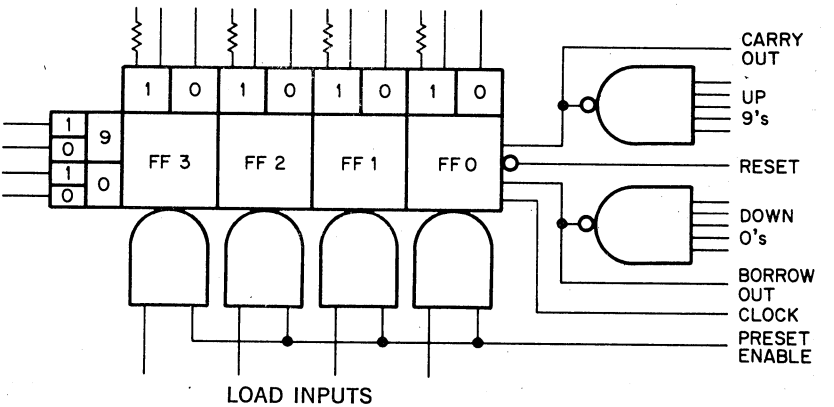
**Outputs:** Each flip flop output (1 or 0) can drive 8 unit loads. Carry Out can drive 10 unit loads. Each inverter output can drive 30 unit loads.

**Power:** +5.0 volts, 217 ma. (max.)

M211 — $69

# BCD UP/DOWN COUNTER
M213

**M SERIES**




| PIN | A CONNECTOR | | B CONNECTOR | |
|---|---|---|---|---|
| | SIDE (1) | SIDE (2) | SIDE (1) | SIDE (2) |
| A | — | +5 | — | +5 |
| B | — | — | — | — |
| C | — | Ground | — | Ground |
| D | 9 (0) Out | 9 (1) Out | 0 (0) Out | 0 (1) Out |
| E | 9 In | Up | 0 In | Down |
| F | 9 In | 9 In | 0 In | 0 In |
| H | Carry Out | 9 In | Borrow Out | 0 In |
| J | Test Point | 9 In | — | 0 In |
| K | — | 9 In | — | 0 In |
| L | — | 9 In | — | 0 In |
| M | Test Point | Preset Enable | — | |
| N | — | Clock | Test Point | Reset |
| P | Test Point | Load FF 0 | Test Point | Load FF 2 |
| R | Test Point | Load FF 1 | Test Point | Load FF 3 |
| S | FF 0 (0) | FF 0 (1) | FF 2 (0) | FF 2 (1) |
| T | Ground | FF 0 (1) | Ground | FF 2 (1) |
| U | FF 1 (0) | FF 1 (1) | FF 3 (0) | FF 3 (1) |
| V | — | FF 1 (1) | — | FF 3 (1) |

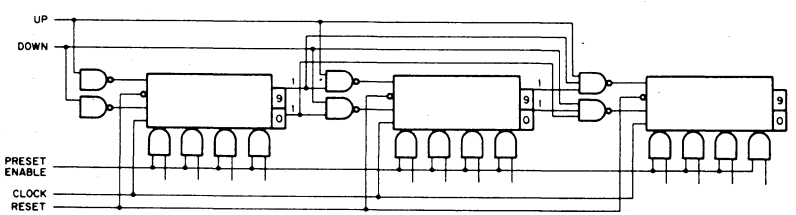
The M213 can be used to construct multi-digit synchronous counters for up/down counting in binary coded decimal. The maximum counting rate is 5 MHz. The counting direction is controlled by enabling the up or down control gate inputs. For maximum noise immunity, the up and down control lines should be kept low until counting is desired. Clock pulses that occur while the up and down lines are both low will not change the contents of the counter. Unpredictable operation will result if both the up and down lines are high at the same time. Positive clock pulses should not occur sooner than 50 ns after any change in the up or down control lines.

The "1" side of each flip-flop output is available directly for controlling nearby logic or through an isolation resistor when decoding displays are being driven at the end of long lines.

The counter may be preset by first resetting the counters and enabling the preset line. The clock input should then be pulsed once with a positive pulse to transfer data from the load inputs into the flip-flops. The up and down control lines must both be low for correct preset operation.

**Counter Construction:** The up and down input gate wiring for cascading M213 modules makes it possible to construct the hardware for fixed decimal point counters so that additional digits to the left or right of the decimal point can be added later as options. If the sockets are wired initially for a larger counter than is thought to be required, the unused high order digits may be left blank. Unused low order digit sockets should have pins AD2 and BD2 connected to +3 volts. When it is found that additional counter capacity or accuracy is needed, M213 modules can be plugged into the blank sockets on either side of the decimal point as required.

The diagram below shows how to connect three M213 counters for up/down counting. Notice that all the counters are clocked at the same time, but that a counter will not count unless the counters of lower significant digits all contain 9's for up counting or 0's for down counting. All unused module inputs should be connected to +3 volts.



**Inputs:** The input loads presented are:

| | |
|---|---|
| CLOCK | — Eight unit loads |
| RESET | — Eight unit loads |
| PRESET ENABLE | — Four unit loads |
| All other inputs | — One unit load |

Pulse widths required:

| | | |
|---|---|---|
| CLOCK | POSITIVE | > 20 nsec |
| RESET | NEGATIVE | > 25 nsec |

**Outputs:** Output drive ability:

| | |
|---|---|
| FLIP-FLOP 1 or 0 | — Seven unit loads |
| FLIP-FLOP 1 (Resistor) | — Five unit loads |
| (Total load on a 1 output is 7 unit loads.) | |
| CARRY OUT | — Eight unit loads |
| BORROW OUT | — Eight unit loads |

**Cascade Outputs:**

| | |
|---|---|
| 9 (1), 9 (0) | |
| 0 (1), 0 (0) | Ten unit loads |

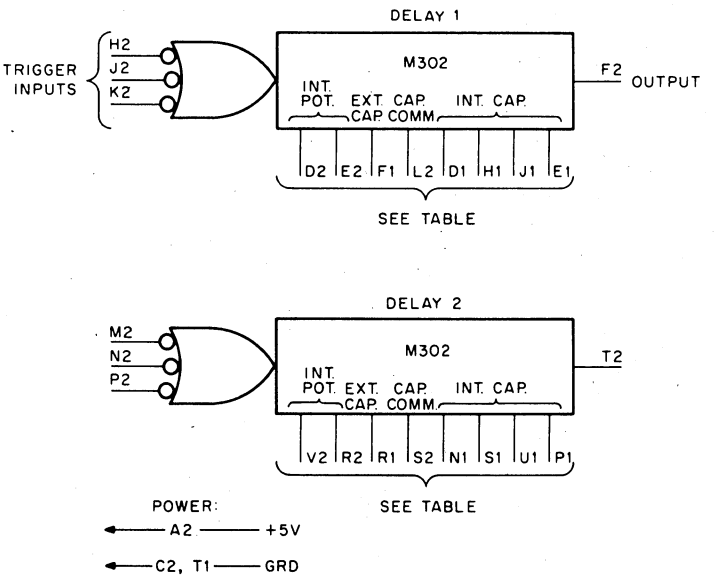
**Power:** +5 volts at 160 ma. (max.)

M213 — $86

Discrete components for DIGITAL Modules are positioned and crimped in place at rates up to 2,200 per hour on pantograph controlled inserting machines. Board layouts are placed in rows, minimizing the effort required to follow the template. Several templates for each module type are generated by numerically controlled milling machines.

# DUAL DELAY MULTIVIBRATOR
M302

**M SERIES**




The M302 contains two delays (one-shot multivibrators) which are triggered by a level change from high to low or a pulse to low whose duration is equal to or greater than 50 nanoseconds. When the input is triggered, the output changes from low to high for a predetermined length of time and then returns to low. The basic DELAY RANGE is determined by an internal capacitor. The delay range may be increased by selection of additional capacitance which is available by connecting various module pins or by the addition of external capacitance. An internal potentiometer can be connected for fine delay adjustments within each range or an external resistance may be used. If an external resistance is used, the combined resistance of the internal potentiometer and the external resistance should be limited of 10,000 ohms.

The fall time of the input trigger should be less than 400 nonoseconds.

The delay time is adjustable from 50 nanoseconds to 7.5 milliseconds using the internal capacitors and can be extended by adding an external capacitor.

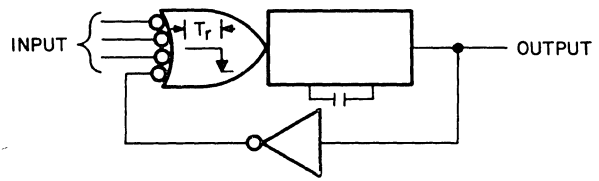
Care should be exercised in the selection of external capacitors to assure low leakage as leakage will affect the time delay.

Recovery time is determined by the size of the capacitance used. The minimum recovery time of this module is 30 nanoseconds when not using any additional capacitance. Recovery time with additional capacitance can be calculated using the formula:

$T_r = 300\ C$

Where $T_r$ is in seconds
C is in farads

Recovery time is defined for this module as follows: Recovery time, $T_r$, is the minimum time interval which must exist before each trigger with all inputs high and the output low. The figure shown below illustrates these conditions:




| Delay Range | Capacitor Value | Interconnections Required | |
|---|---|---|---|
| | | Delay 1 | Delay 2 |
| 50 nsec — 750 nsec | 100 pf (internal) | None | None |
| 500 nsec — 7.5 usec | 1000 pf (internal) | D1 — L2 | N1 — S2 |
| 5 usec — 75 usec | 0.01 uf (internal) | H1 — L2 | S1 — S2 |
| 50 usec — 750 usec | 0.10 uf (internal) | J1 — L2 | U1 — S2 |
| 500 usec — 7.5 msec | 1.0 uf (internal) | E1 — L2 | P1 — S2 |
| Above 7.5 msec | Add external capacitors between specified pins | F1 — L2 | R1 — S2 |
| **Adjustable Delays:** connect pins to add internal adjustment potentiometer. Without a potentiometer, the delay will not recover. An external potentiometer of less than 10KΩ can be used by connecting it between E2 or R2 and ground pin C2. Use of an external adjustment resistor will cause some increase in jitter. It is recommended that leads to an external potentiometer be twisted pairs and as short as possible. | | D2 — E2 | V2 — R2 |

**Inputs:** Each input presents 2½ unit loads.

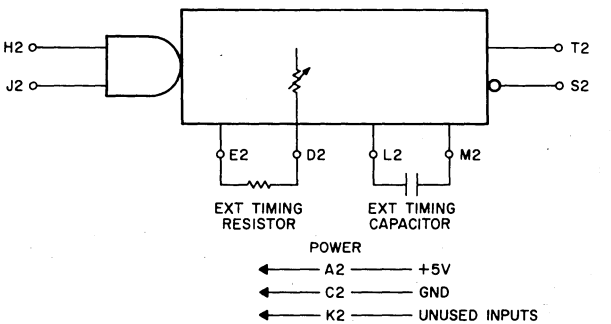
**Outputs:** Each output is capable of driving 25 unit loads.

**Power:** +5 volts, 166 ma. (max.)

M302 — $46

# INTEGRATING ONE SHOT
## M306

**M SERIES**




The M306 contains one integrating monostable multivibrator mounted on a single flip-chip ™ module.

**TIMING CAPACITORS**

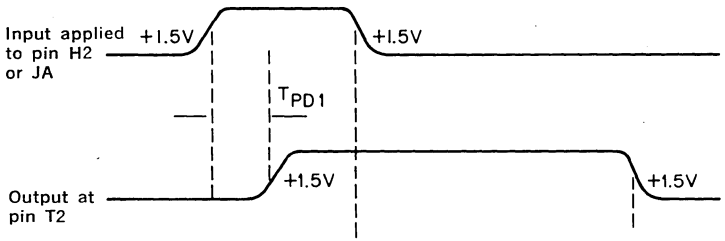
Course adjustment of the integration period is accomplished by customer supplied capacitors which may be attached to module pins L2 and M2. When using polarized capacitors, the positive terminal should be connected to pin M2. Two split lugs are also provided on the module for those customers who would like to permanently install the capacitor on the module itself. The minimum equivalent parallel resistance of capacitor leakage should always exceed 250K ohms.

**TIMING RESISTANCE**

Fine adjustment of the timing period may be accomplished by a multiturn potentiometer provided on the module. Provision is also made to allow the customer to connect an external timing resistor or potentiometer between pins D2 and E2. When an external potentiometer is used, care should be taken to prevent the coupling of externally generated electrical noise into the module. The maximum resistance of the timing resistance, including the internally provided potentiometer, should not exceed 25,000 ohms. If an external timing resistor is not used, pins D2 and E2 must be connected together.

**TIMING PERIOD**

The operation of the M306 is illustrated in the timing diagram shown below:




The integration period is measured from the trailing edge of the input pulse to the trailing edge of the output pulse. The approximate integration time may be calculated by the following:

$$t \simeq .87\ (R + 700\ \Omega)\ (C + 175 \times 10^{-12}\ F)$$

where R is in ohms and C is in farads. The width of the input pulse is independent of the integration time. An input pulse of 30NS will trigger the M306.

**STABILITY**

The inherent temperature stability of the M306 is normally −.06% °C, exclusive of the temperature coefficient of the timing capacitor.

**Inputs:** Each Input represents 1.25 unit loads

**Outputs:** Pin S2 will supply 12.5 unit loads. Pin T2 will supply 11 unit loads.

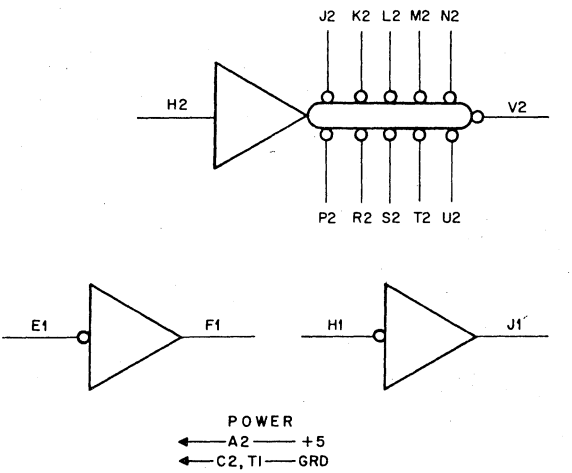
Pin K2 is a source of Logic "1" used to return unused inputs. It will supply 10 unit loads. The minimum pulse width is 225NS and maximum pulse width is limited only by capacitor leakage (40sec is a typical maximum)

**TPD1** = 40NS Max.

**POWER:** +5 volts at 120 ma. (max.)

# DELAY LINE
## M310

**M SERIES**




The M310 consists of a tapped delay line with associated circuitry and two pulse amplifiers. The total delay is 500 nanoseconds with taps available at 50 nanosecond intervals.

The time delay is increased when the amplifier is connected to the delay line taps in ascending order as follows: J2, K2, L2, M2, N2, P2, R2, S2, T2, U2, and V2. The tap J2 yielding the minimum delay and the tap V2 yielding the maximum delay.

The pulse amplifiers are intended to be used to standardize the outputs of the delay line. The output of the pulse amplifier is a positive pulse whose duration is typically 50 to 200 nanoseconds. These amplifiers are not intended to be driven by TTL IC logic.

**Inputs:** Pin H2 represents 2.5 TTL unit load.

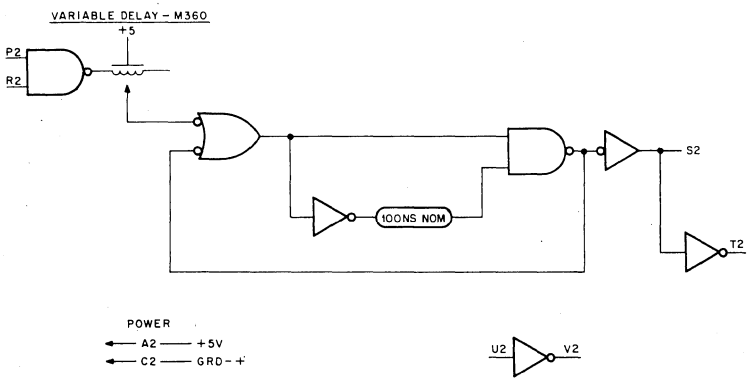
**Outputs:** Pin F1 and J1 outputs can drive 30 unit loads.

**Power:** +5 volts at 89 ma. (max.)

M310 — $58

# VARIABLE DELAY
## M360

**M SERIES**




The M360 contains an adjustable delay line with a standardizing amplifier. The delay is adjustable between the limits of 50 nanoseconds to 300 nanoseconds by means of a slotted screw which is accessible from the handle end of the module. The resolution of the delay adjustment is approximately 1 nanosecond. The output consists of a positive pulse whose width is nominally 100 nanoseconds and the leading (positive going voltage) edge of which, is delayed with respect to the leading (positive going voltage) edge of the input by a length of time as determined by the setting of the delay line adjustment.

**Inputs:** Pins P and R represent one TTL unit load. Pin U represents two TTL unit loads.

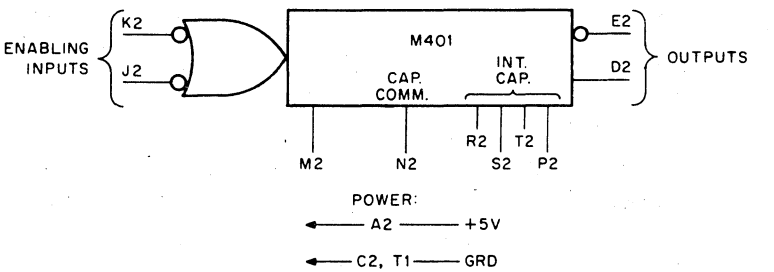
**Outputs:** Pin S can drive 27 TTL unit loads. Pins T and V are outputs consisting of open collector NPN transistors and can sink 30 milliamperes to ground. Voltage applied to Pins T and V must **not** exceed +20 volts.

**Power:** +5 volts, 50 ma. (max.)

M360 — $68

# VARIABLE CLOCK
## M401

**M SERIES**




M401 VARIABLE CLOCK

The M401 Variable Clock is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

The module is intended for use as the primary source of timing signals in a digital system. Repetition rate is adjustable from 175 HZ to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A two-input OR gating input is provided for start-stop control of the pulse train. A level change from high to low with fall time less than 400 nsec is required to enable the clock.

Enabling inputs to output E2 is 50 nanoseconds.

| Frequency Range | Interconnections Required | |
|---|---|---|
| 1.5 MHz to 10 MHz | (100 pf) | NONE |
| 175 KHz to 1.75 MHz | (1000 pf) | N2 — R2 |
| 17.5 KHz to 175 KHz | (.01 μfd) | N2 — S2 |
| 1.75 KHz to 17.5 KHz | (0.1 μfd) | N2 — T2 |
| 175 Hz to 1.75 KHz | (1.0 μfd) | N2 — P2 |

**Fine Frequency Adjustment:**
Controlled by an internal potentiometer. No provision is made for any external connections.

External capacitor may be added by connection between pin N2 and ground.

The M401 may also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision "E" or later. The voltage applied to Pin M should be limited to the range of 0 volts to +10.0 volts. This voltage swing will allow the frequency to be shifted by approximately 30 percent in the frequency range using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 ufd. If the voltage applied to Pin M is D.C. or low frequency (below 1 KHz), Pin M will appear approximately as a +1.0 volt source with a Thevenin resistance of 800 ohms. Modulating the M401 with a 10V P-P signal about a center frequency, as derived by the application of a mean voltage of +5 volts to Pin M, will yield a typical frequency excursion in excess of ±15% about the center frequency. Typical frequency excursions which may be obtained are shown below:

| Voltage applied to Pin M | CAPACITOR | | | |
|---|---|---|---|---|
| | 1.0 ufd. | 0.1 ufd. | 0.01 ufd. | .001 ufd. |
| 0 | 1.000 | 10.00 | 100.0 | 1000 |
| +1 | 1.054 | 10.49 | 104.6 | 1036 |
| +2 | 1.101 | 10.94 | 109.2 | 1071 |
| +3 | 1.147 | 11.39 | 113.6 | 1108 |
| +4 | 1.193 | 11.83 | 118.0 | 1142 |
| +5 | 1.238 | 12.26 | 122.2 | 1181 |
| +6 | 1.282 | 12.69 | 126.4 | 1271 |
| +7 | 1.325 | 13.10 | 130.4 | 1295 |
| +8 | 1.368 | 13.50 | 134.2 | 1312 |
| +9 | 1.408 | 13.87 | 137.7 | 1322 |
| +10 | 1.443 | 14.20 | 140.9 | 1323 |
| | | | | Output frequency in KHz |

**Inputs:** Each enable input represents 1 unit load. Pin M, refer to text above.

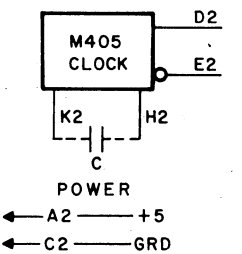
**Outputs:** The output pulse width is 50 nsec. The positive output can drive 10 unit loads; the negative output, 9 unit loads.

**Power:** +5 volts, 80 ma. (max.) using printed circuit board revision "E" or later.

M401 — $55

# CRYSTAL CLOCK
## M405

**M SERIES**




The M405 clock employs a series resonant crystal oscillator to obtain a frequency stability of .01% of specified value between 0°C and +55°C. The clock frequency may be specified anywhere in the range of 5 KHz to 10 MHz by the customer.

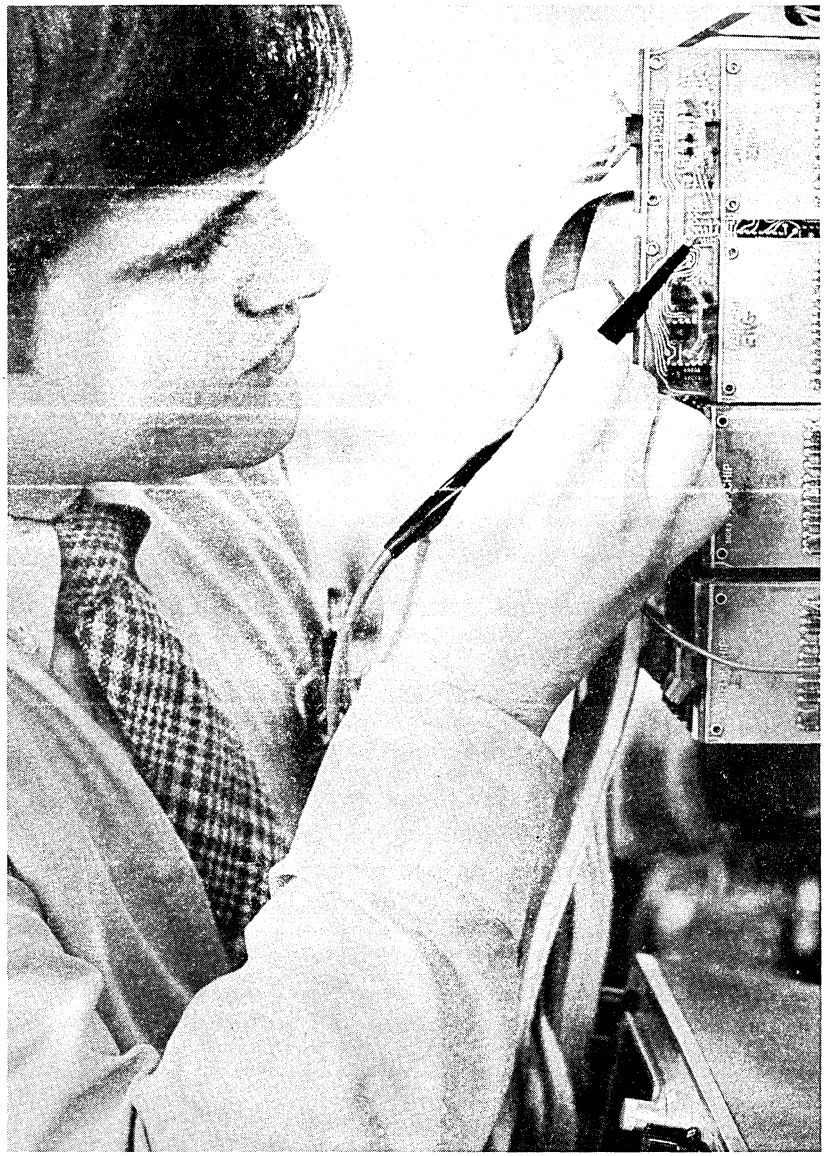
**Outputs:** Outputs at pins D2 and E2 are respectively positive and negative going 0-+3 volt 50 nsec pulses. Pin D2 can drive 10 unit loads while E2 can drive only 9 unit loads. Pulses at pins D2 and E2 are time shifted by one gate delay with negative pulse at pin E2 leading the positive pulse at D2 by a maximum of 20 nsec. The output pulse width can be modified by the addition of an external capacitor between pins K2 and H2. This capacitor will increase the output pulse width by approximately 1 nsec per 2.5 mmfd of additional capacitance.

**Power:** +5 volts, 50 ma. (maximum)

**Ordering Information:** When ordering the M405 always specify frequency. Allow six weeks for delivery.

**Standard Stock Frequencies:** 1.333 MHz, 2.000 MHz, 5.000 MHz.

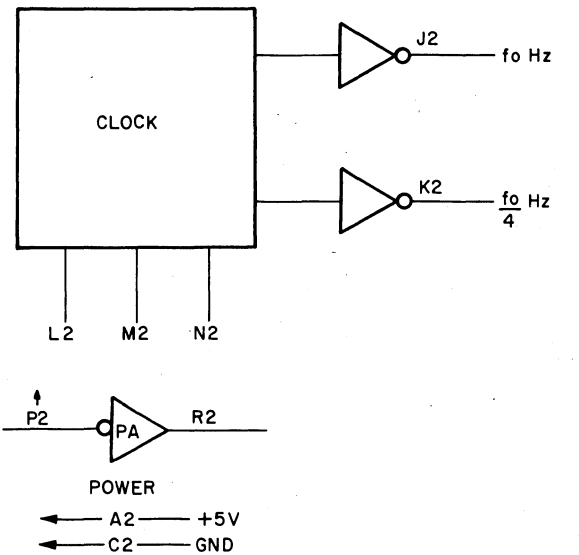
M405 — $100



DEC's PDP-14 is designed to be more reliable, more flexible and, in most cases, less expensive than any other electrical system now available for control of machines and systems utilizing two state devices such as limit switches, pushbuttons, motor contactors and solenoids.

# REED CLOCK
## M410

**M SERIES**




The M410 is a free-running contactless-resonant-reed-tuned clock which provides stable timing signals for a system using the M706 and M707 teletype converter modules. Overall frequency stability of the outputs is better than .1% in the temperature range 0°C-70°C. Available clock frequencies are listed below. A pulse amplifier is provided for the generation of nominal 150 nsec pulses.

**Available Frequencies:** (fo in HZ) = 400 (50 baud), 550, 600 (75 baud), 750, 880 (110 baud), 1200 (150 baud), 1800, 2000, 2200, 2400 (300 baud).

**Inputs:** The pulse amplifier input presents one unit load.

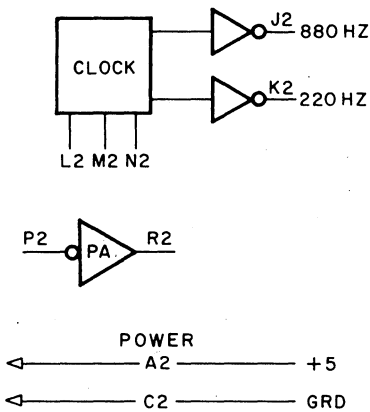
**Outputs:** Pin J2 drives 30 unit loads at fo. Pins N2 and M2 drive 9 unit loads at fo/2. Pin L2 drives 9 unit loads at fo/4. Pin K2 drives 30 unit loads at fo/4. Pin R2 drives 10 unit loads with a nominal 150 nsec positive output pulse. Under normal operating conditions, pins L2, M2, N2, are used as test points.

**Power:** +5 volts at 95 ma. (max.)

M410 — $70

# VARIABLE CLOCK
M452

**M SERIES**




The M452 is a free running clock which generates the necessary timing signals for the PDP 8/I teletype control. Frequency adjustment of this module is limited to less than 5% and the overall clock stability with respect to supply voltage and temperature variations is about 1%. The available output frequencies are 880Hz, and 220Hz. A pulse amplifier is provided for the generation of nominal 150 nsec pulses.

**Inputs:** The pulse amplifier input presents one unit load.

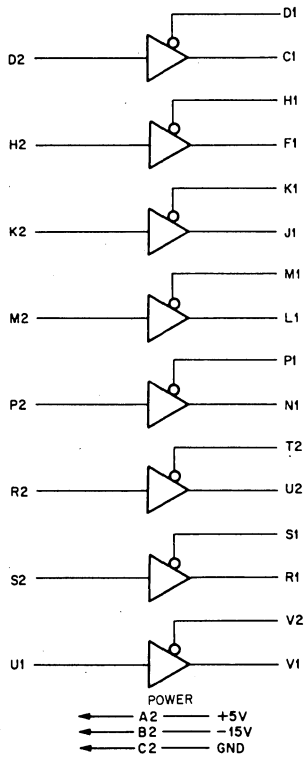
**Outputs:** Pin J2 drives 30 unit loads at 880Hz. Pins N2 and M2 drive 9 unit loads at 330Hz. Pin L2 drives 9 unit loads at 220Hz. Pin K2 drives 30 unit loads at 220Hz. Pin R2 drives 10 unit loads with a nominal 150 nsec positive output pulse. Under normal operating conditions, pins L2, M2, N2, are used as test points.

**Power:** +5 volts, 77 ma. (max.)

M452 — $40

# NEGATIVE INPUT POSITIVE OUTPUT RECEIVER
## M500

**M SERIES**




The M500 module is used to convert negative input signals to positive output signals. Each card contains 8 converters and is pin compatible with the M510 positive receiver card.

A ground input at D2 will yield a +3 at D1 and ground at C1. The propagation delay is 40 nsec. Do not connect to pin E2 (used for manuf. test only).

**Inputs:** 1 ma. at ground; 0 ma. at −3 volts

Input switching level is normally −1.5 volts. The maximum input voltage is −3 volts.

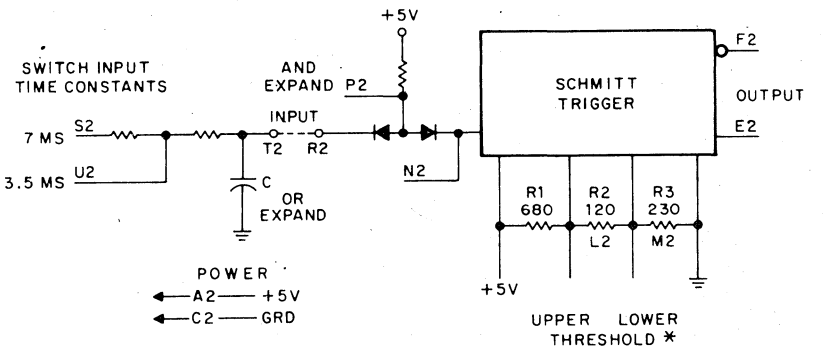
**Output:** Each output is capable of driving 10 unit loads.

**Power:** +5 volts at 160 ma. (max.); −15 volts at 64 ma. (max.)

M500 — $55

# SCHMITT TRIGGER
## M501

**M SERIES**

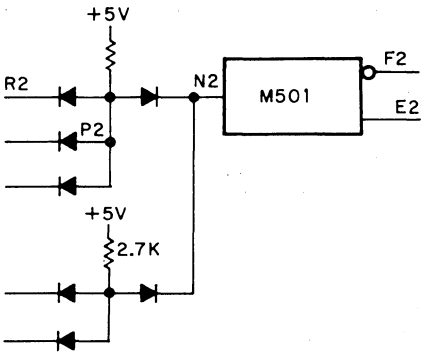



Basically a Schmitt Trigger with variable thresholds, the M501 is used as a Switch Filter, Pulse Shaper and Threshold Detector. Complementary positive logic levels are provided as outputs.

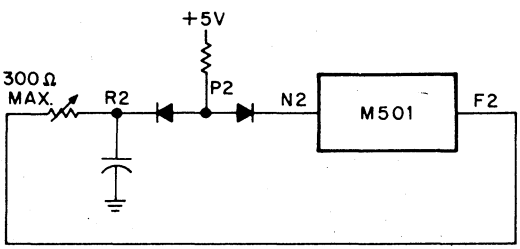
The INPUT on PIN R2 is compared with the thresholds set on PINS L2 and M2, Upper and Lower respectively. AND and OR EXPANSION may be performed on PINS P2 and N2. Module R001 and R002 provide the diodes required. An integrator is provided on the input, allowing SWITCHES to be connected to the Schmitt Trigger with contact bounce effects eliminated. Two switch TIME CONSTANTS are provided. Inputs to PIN S2 result in a 7 m sec TIME CONSTANT, to PIN U2, 3.5 m sec.

The Upper and Lower threshold are preset at 1.7 volts and 1.1 volts. They may be modified by the addition of resistor combination in parallel with the internal network. However, the upper threshold must not exceed 2.0 volts or the lower threshold fall below 0.8 v.

| | | | | |
|---|---|---|---|---|
| $R_x$ | PARALLEL | R2 | — | THRESHOLD CLOSER |
| $R_x$ | PARALLEL | R1 | — | UPPER RISES |
| $R_x$ | PARALLEL | R3 | — | LOWER FALLS |




Connecting a resistor from OUTPUT PIN F TO INPUT PIN R with PIN T tied to PIN R forms an oscillator.




**Inputs:** Input signal swing on PIN R2 is limited to ±20 volts.

**Input Pin R2:** 2.7 KΩ to +5 volts or 1.8 ma. at ground.

**Pin P2**—AND EXPAND input
**Pin N2**—OR EXPAND input
**Pin S2**—RC SWITCH INPUT Filter 7 msec
**Pin U2**—RC SWITCH INPUT Filter 3.5 msec
**Pin L2, M2**—Available for threshold modification.

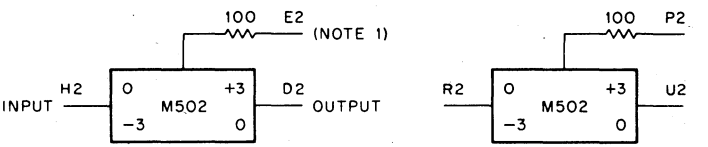
**Outputs:** PIN F2 goes to GROUND when the input on PIN R2 rises above the UPPER threshold, having been below the lower threshold.
PIN F2 rises to +3 volts when the input on PIN R2 falls below the LOWER threshold, having been above the upper threshold.
PIN E2 is the complement of the PIN F2.
PIN E2 can drive ten unit loads.
PIN F2 can drive eight unit loads.

**Power:** +5 volts at 31 ma. (max.)

M501 — $25

# NEGATIVE INPUT CONVERTER
## M502

**M SERIES**

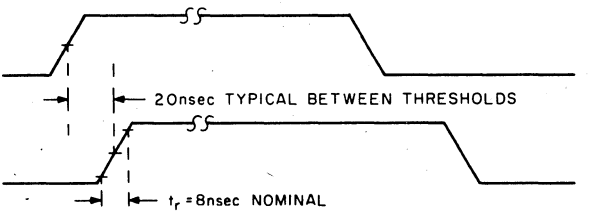



POWER:

A2 — +5V
B2 — −15V
C2, M2 — GRD

NOTE

1. CONNECT TO OUTPUT WHEN NOT DRIVING 92ohm COAX.




M502 NEGATIVE INPUT CONVERTER

| INPUT | OUTPUT |
|---|---|
| 0v | +3v |
| −3v | 0v |

The M502 contains two non-inverting high-speed signal converters which interface standard negative (—3v and ground) DIGITAL logic levels or pulses with M and K Series positive logic mocules. These converters provide sufficient current drive at a low output impedance for system interconnections by means of terminated 92-ohm coaxial cable. The converters operate at frequencies up to 10 MHz, with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec.

**Inputs:** Input loading is equivalent to a 3 ma. clamped load.

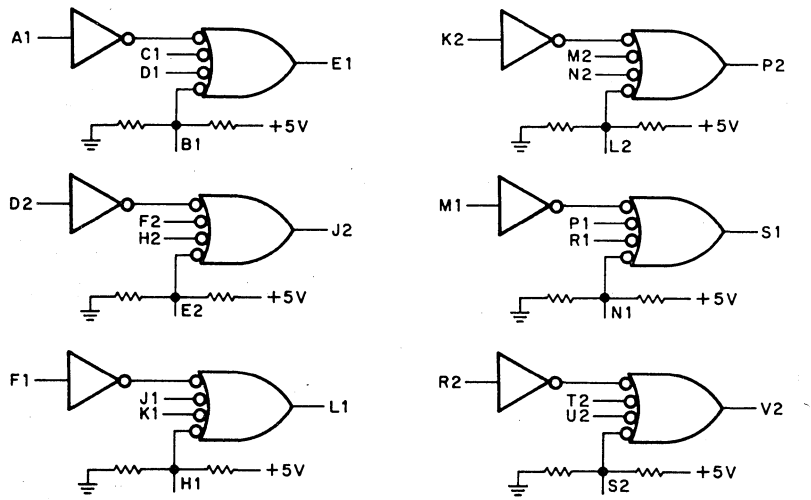
**Outputs:** Each output can drive terminated 92-ohm coaxial cable, and supply an additional 30 ma. at +3 volts or sink an additional 30 ma. at ground. Output rise and fall times depend on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds are increased by connecting the 100 ohm resistor to the output.

**Power:** +5 volts, 49 ma. (max.); —15 volts, 92 ma. (max.). Add 44 ma. for each 100 ohm resistor connected to outputs.

M502 — $26

# NEGATIVE INPUT CONVERTER
M506

**M SERIES**




The M506 contains six non-inverting signal converters which can be used to interface the negative logic levels or pulses of duration greater than 100 nsec to M and K Series positive logic levels of +3 volts and ground. These converters operate at frequencies up to 2 MHz with typical rise and fall propagation time of respectively 70 nsec and 40 nsec.

In addition, to the negative level inputs, each converter circuit has three additional NOR inputs for positive logic levels of +3 volts and ground. One of these inputs is tied to +3 volts so that unused inputs can be tied to a source of logic 1.

**Inputs:** All negative level inputs (A1, D2, . . . R2) present a 10 ma. at ground load.

Inputs B1, E2, . . . S2 present five TTL unit loads and can drive seven TTL unit loads at logic 1 if not used as an input.
All other inputs present 1 unit load.

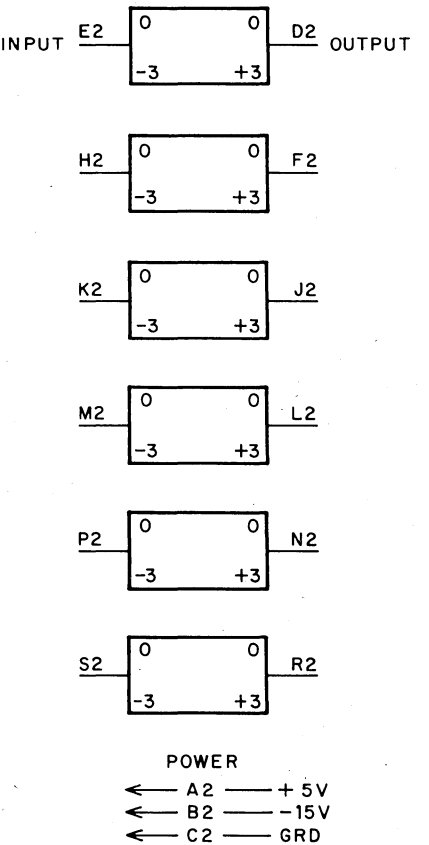
**Outputs:** Each output can drive 10 TTL unit loads.

**Power:** +5 v at 81 ma. (max.); −15v at 115 ma. (max.).

M506 — $52

# BUS CONVERTER
M507

**M SERIES**




**INPUT**
GRD
−3V

**OUTPUT**
GRD
+3V

The M507 contains six inverting level shifters which will accept —3 volts and GRD as inputs. The input to each level shifter consists of a 10 ma. clamped load and is diode protected against positive voltage excursions.

The output consists of an open collector NPN transistor. The output of each level shifter will sink 100 ma. to GRD. The maximum voltage which may be applied to the output is +20 volts. The output transistor is protected against negative voltage excursions by a diode connected between the collector and GRD. The output rise is delayed by 100 nsec. for pulse spreading.

The principle use of this module is to convert negative voltage logic levels or pulses of duration greater than 100 nsec.

**Inputs:** Input loading is equivalent to a 3 ma. clamped load.

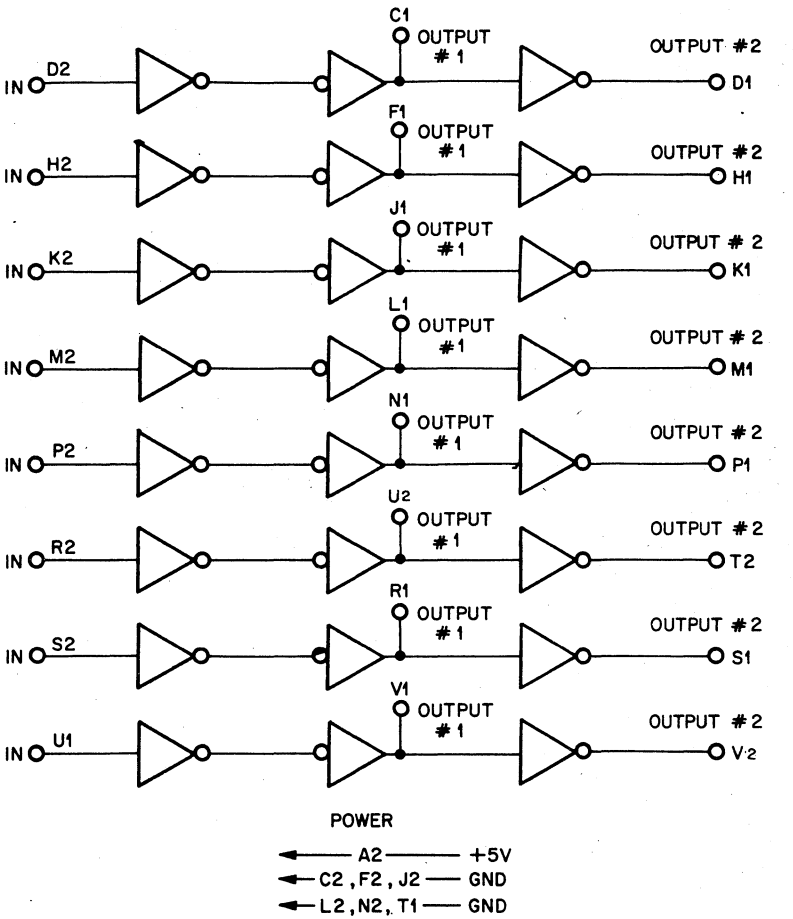
**Outputs:** Each output can sink 100 ma. to GRD. Maximum voltage applied to any output is +20 volts.

**Power:** +5 volts, 42 ma. (max.); —15 volts, 115 ma. (max.).

M507 — $45

# I/O BUS RECEIVER
M510

**M SERIES**




The M510 is a positive input/output receiver card for use with the PDP15. It contains 8 high input impedance circuits of at least 27 KΩ and input switching thresholds of about +1.5 volts. Each receiver has two outputs, one of the same polarity as the input, the other, the inverse of the input. The receiver card can be used anywhere on the I/O Bus, but power (B+) must be applied at all times, since the input impedance drops to 1 KΩ when power is off. Do not connect to pin E2 (used for manuf. test only).

**Inputs:** The input impedance is 27 Ω (min.). Each input load current is 80 ma. (max.) and the threshold switching level is 1.4 to 1.6 volts.

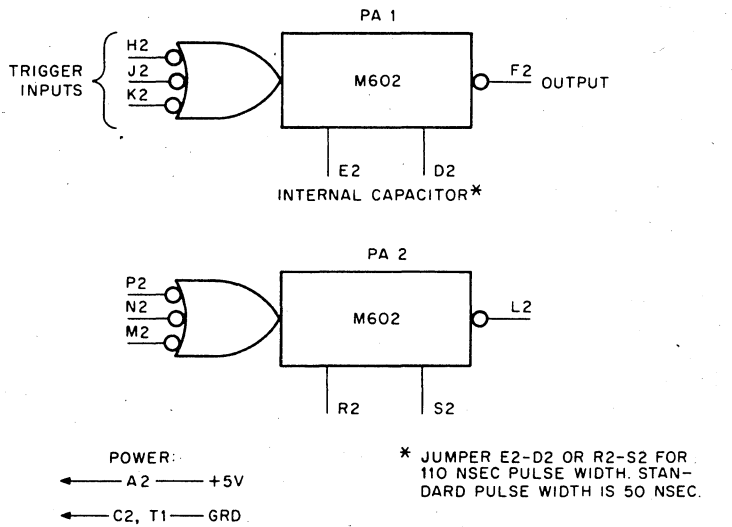
**Outputs:** Output #1 fan out = 9 unit loads. Output #2 fan out = 10 unit loads. Output #2 delay = 50 nsec (from input)

**Power:** +5 volts at 170 ma. (max.)

M510 — $51

# PULSE AMPLIFIER
## M602

**M SERIES**



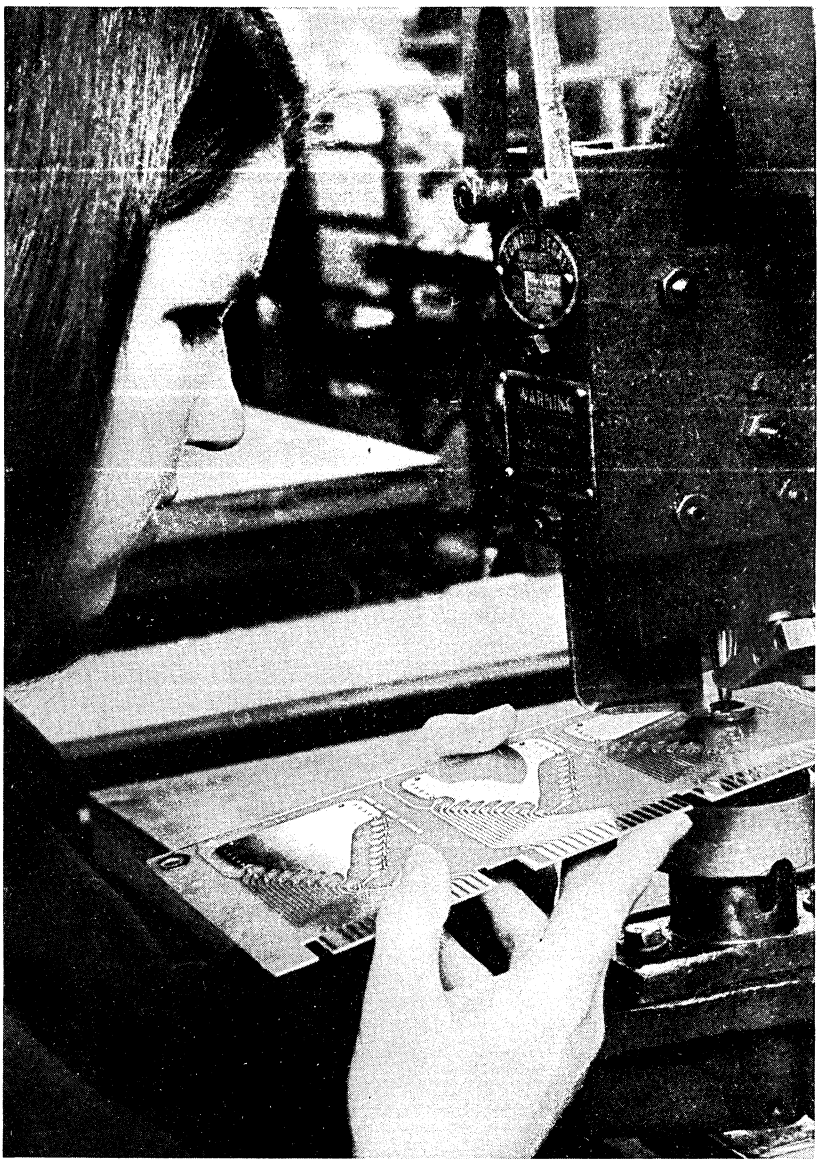

The M602 contains two pulse amplifiers which provide power amplification, standardize pulses in amplitude and width, and transform level changes into a standard pulse. A negative pulse output is produced when the input is triggered by a transition from high to low. Propagation time between input and output thresholds is 30 nsec maximum. An internal capacitor is brought out to pin connections to permit the standard 50 nsec output pulse to be increased to 110 nsec (nominal). Recovery time is equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 nsec and must remain below 0.8 volts for at least 30 nanoseconds. Maximum PRF is 10 MHz.

**Inputs:** Each input presents 2½ unit loads.

**Outputs:** Each output is capable of driving 30 unit loads.

**Power:** +5 volts, 213 ma. (max.)

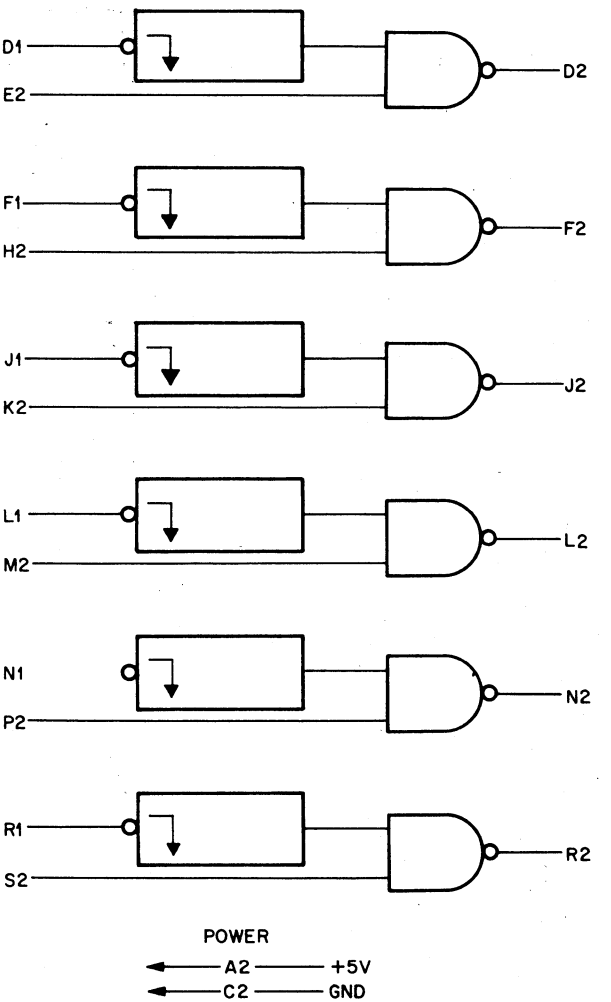
M602 — $28



DEC's Module Assembly inserts rivets and eyelets into printed circuit boards before beginning component insertion production.

# PULSE GENERATOR
M606

M
SERIES




The M606 contains six pulse generators. Each circuit will produce a pulse to ground upon the application of a level shift from high to low to the input. The time duration of the output pulse will be at least 30 nsec. but no longer than 100 nsec. Each circuit contains an inhibit input. The output will be inhibited when the inhibit input is grounded. If this input is not used, it should be tied to a logic 1 level.

The M606 may be used for setting or clearing of flip-flops by applying the output of the M606 to the direct clear or set inputs of up to 14 flip-flops.

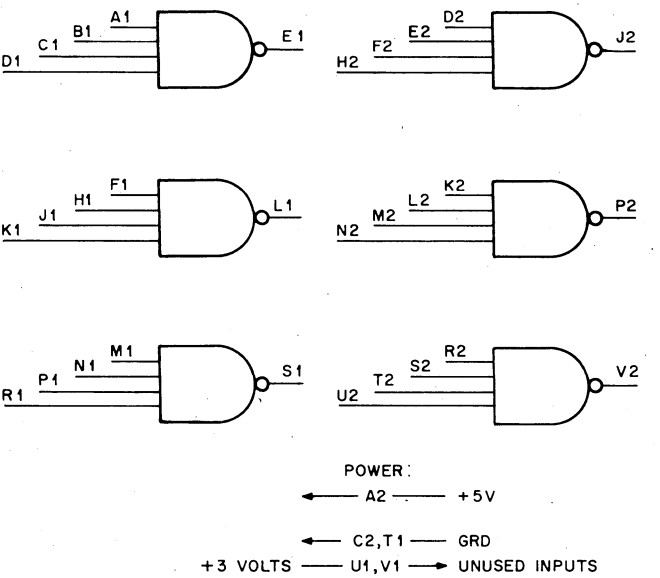
**Inputs:** Pins D1, F1, J1, N1, and R1 represent two unit loads. Pins E2, H2, K2, M2, P2, and S2 represent one unit load.

**Outputs:** All outputs may drive 28 unit loads and consists of a ground level with a time duration of at least 30 nsec. but not greater than 100 nsec. Pin V1 is a source of logic 1 and may supply ten unit loads.

**Power:** +5 volts at 188 ma. (max.)

# FOUR-INPUT POWER NAND GATE
M617

**M SERIES**




M617 POWER NAND GATE

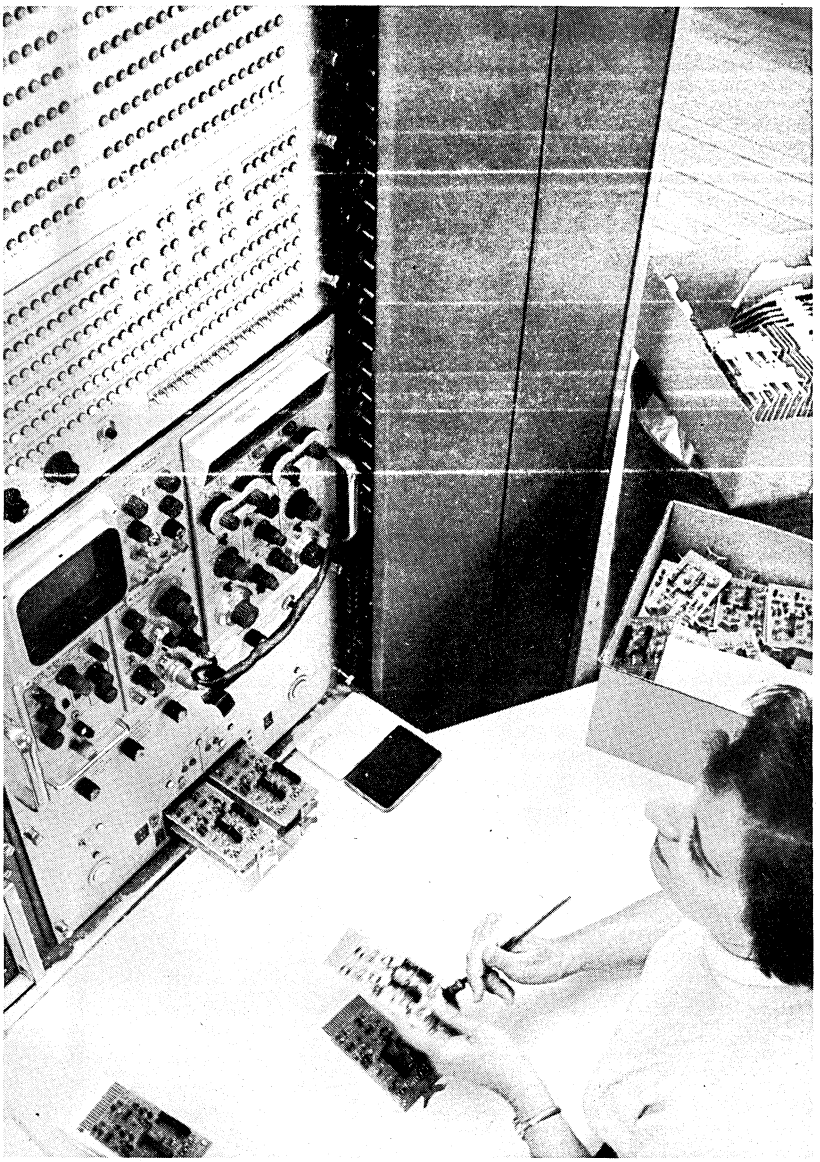
The M617 contains 6 four-input NAND gates each capable of driving up to 30 unit loads. Typical gate propagation delay is 15 nsec. Physical configuration and logical operation are identical to the M117.

**Inputs:** Each input presents 1 unit load.

**Outputs:** Each output is capable of driving 30 unit loads.

**Power:** +5 volts, 97 ma. (max.).

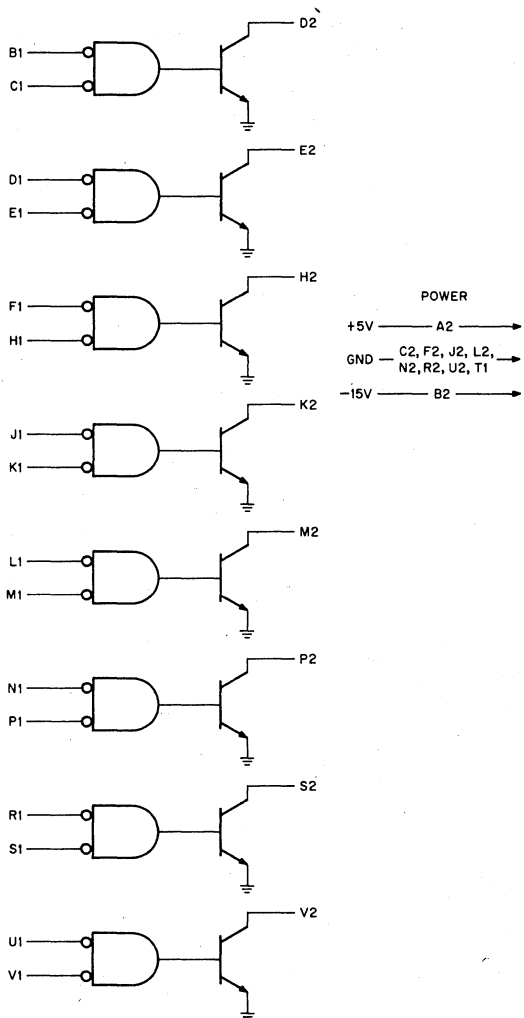
M617 — $26



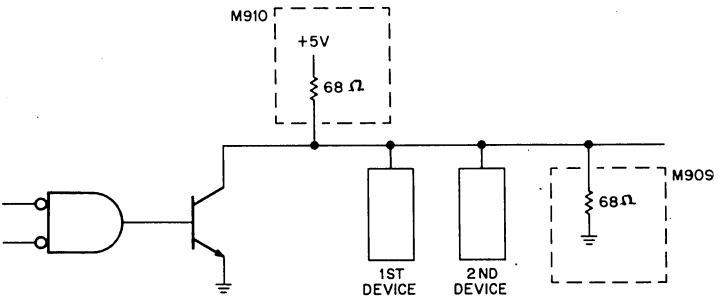
DEC thoroughly tests all finished modules, performing 100 ac and dc tests in less than 5 seconds. Most testing is done automatically on one of three computer-operated test stations like this one.

# EIGHT BIT POSITIVE INPUT/OUTPUT BUS DRIVER
## M622

**M SERIES**



The M622 contains eight two input AND gate bus drivers for convenient driving of the positive input bus of the PDP-15. The output consists of an open collector NPN transistor.




Pull up resistors of 68Ω to +5.0 volts (supplied on M910) must be tied to the output and the last device should terminate all lines to ground with a 68Ω resistor (supplied on M909).

**Inputs:** Each input presents 1.25 TTL unit loads.

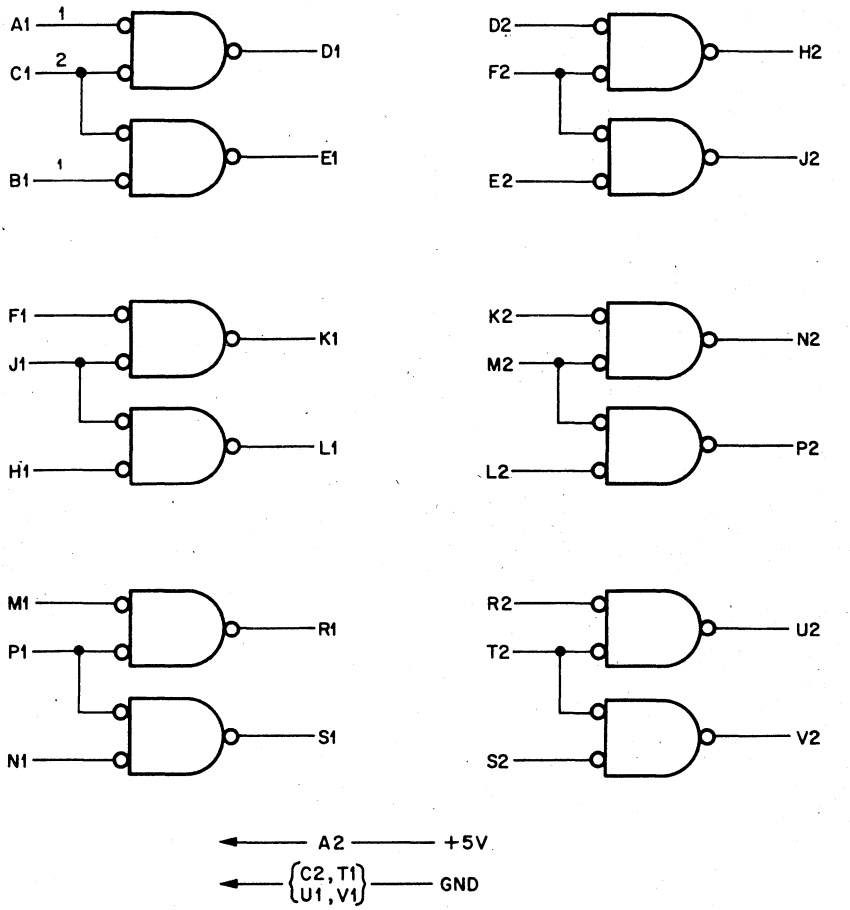
**Outputs:** The maximum voltage applied to the output transistor must not exceed +20 volts and the collector current must not exceed 100 ma. The propagation time is 25 nsec.

**Power:** +5 volts, 210 ma. (max.) excluding output current.

M622 — $45

# BUS DRIVER
## M623

**M SERIES**




The M623 contains twelve two input AND gate bus drivers for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. Each driver can sink 100 ma. at ground and allows a maximum output voltage of +20 volts. The output consists of an open collector NPN transistor.

**Inputs:** Input levels are standard TTL levels of 0 volts and +2.4 volts. Data inputs A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2, and S2 each present one TTL unit load. All other inputs present two unit loads.

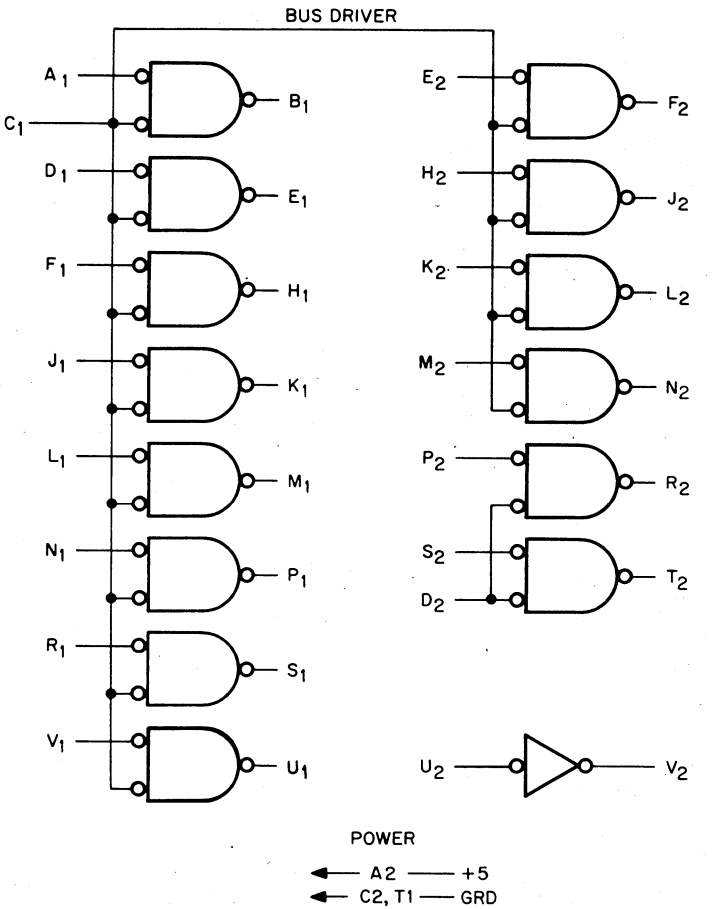
**Outputs:** A driver output will be at ground when both inputs are at ground. Output rise and fall (TTT) are typically 30 nsec when a 100 ma. resistive load is connected to a driver output. Output voltage must not exceed +20 volts.

**Power:** +5 volts, 71 ma. (max.) plus external load.

M623 — $40

# BUS DRIVER
## M624

**M SERIES**




The M624 contains fifteen bus drivers intended for convenient driving of the positive input bus of either the PDP-8I or PDP-8L. Twelve of the drivers have a common gate line and would be used for DATA. There are three additional drivers, two of which share a common gate line and the third without a gate line. These three additional drivers were intended to accommodate the functions of "Program Interrupt", "IO Skip" and "Clear AC".

**Inputs:** Pin C1 presents 12 TTL unit loads.
Pin D2 and U2 present two unit loads.
All other input pins present one unit load.

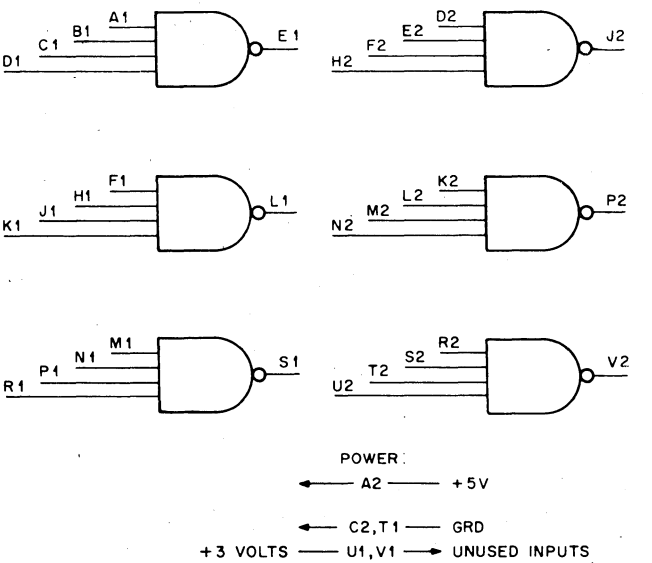
**Outputs:** All outputs can sink 100 ma. to ground. Voltage applied to the output should be equal to or less than +20 volts. The output consists of an open collector NPN transistor. Output rise and fall TTT are typically 30 nanoseconds when a 100 ma. resistive load to +5.0 volts is connected to a driver output.

**Power:** +5 volts, 89 ma. (max.). (Driver outputs not connected).

M624 — $45

# NAND POWER AMPLIFIER
M627

**M SERIES**




M627 NAND POWER AMPLIFIER

The M627 combines power amplification with high-speed gating, specifically for high fan-out of clock or shift pulses to expanded counters and shift registers. Propagation time between input and output transitions is typically 6 nsec. To utilize the timing accuracy of this module, wire runs of minimum length are recommended.

The module may also be used as a four-input NAND gate. In the pulse amplifier application, unused inputs should be connected to the +3 volt pins provided.

**Inputs:** Each input presents 2½ unit loads.

**Outputs:** Each output is capable of driving 40 unit loads.

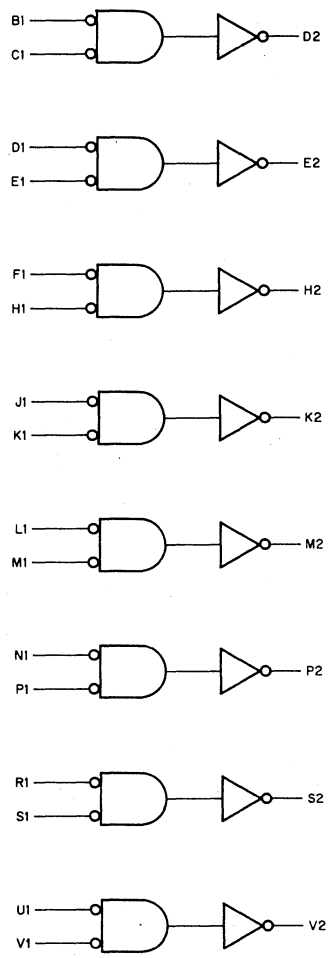
**Power:** +5 volts, 136 ma. (max.)

M627 — $29

Digital's expansion of manufacturing is well underway with plants under construction in Westfield and Westminster and production already in progress at the new pilot plant in Leominster. Shown above is the module production area at the Leominster plant.

# POSITIVE INPUT NEGATIVE OUTPUT BUS DRIVER
## M632

**M SERIES**



The M632 contains eight, two input AND gate bus drivers for convenient driving of the negative bus.

**Inputs:** Each input presents 1.25 TTL unit loads.

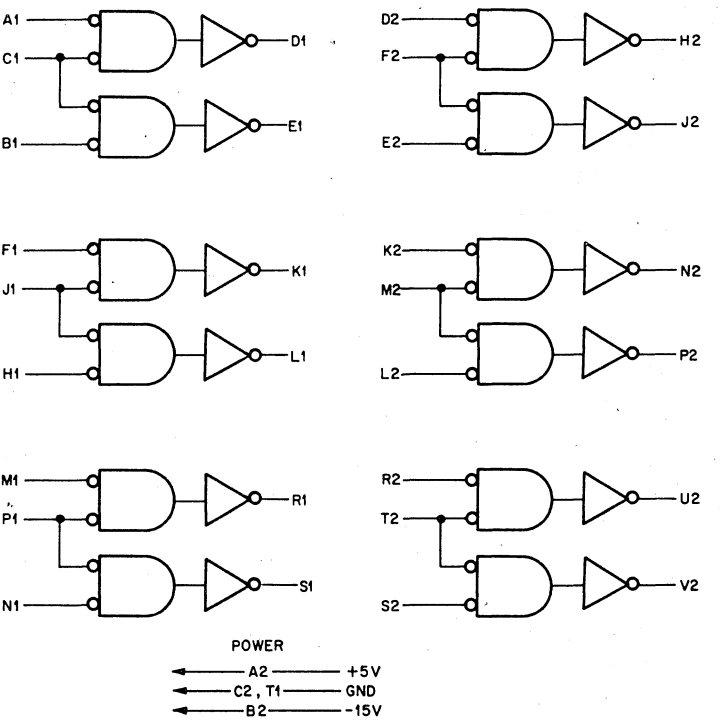
**Outputs:** The output is internally clamped to keep it between −3 volts and ground. The output current must not exceed 100 ma.

The propagation delay is 50 nsec. (Max.)

**Power:** +5 volts, 175 ma. (max.); −15 volts, 40 ma. (max.), excluding output current

# NEGATIVE BUS DRIVER
## M633

**M SERIES**




The M633 contains twelve bus drivers intended for convenient driving of the negative bus of the PDP-8, PDP-8/I. Each driver consists of an open collector PNP transistor. It is pin compatible with the M623 positive voltage bus driver.

**Inputs:** Input levels are standard TTL levels. Data inputs A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2 and S2. Each present one TTL unit load. All other inputs represent two unit loads.

**Outputs:** Open collector PNP transistor capable of supplying 20 ma. from ground. Voltage applied to the output should not exceed −6 volts.

**Conversion:** Logic Diagram: An active voltage is a True State, i.e., −3 v. or +3 v. = "1.". A ground is a True State. Grounded inputs will yield grounded outputs.

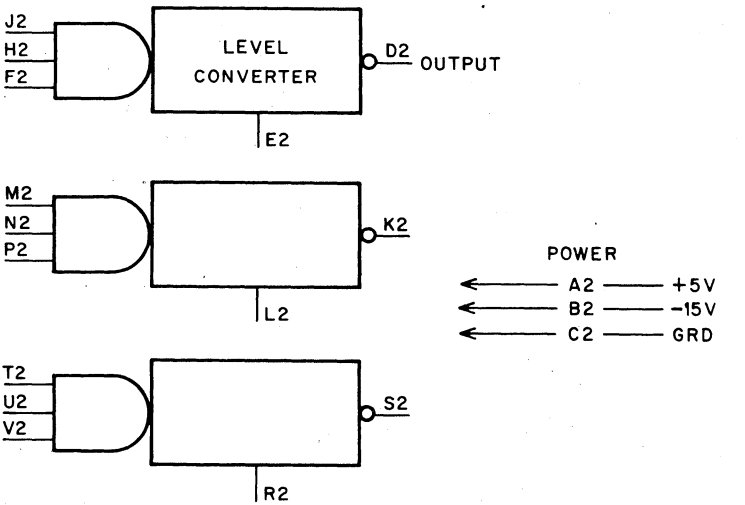
**Propagation Delay:** 40 nsec. typ.

**Power:** +5 volts at 100 ma. (max.); −15 volts at 40 ma. (max.)

M633 — $50

# NEGATIVE OUTPUT CONVERTER
## M650

**M SERIES**




NEGATIVE OUTPUT CONVERTER

0 IN => −3V
+3 IN => 0 OUT

The M650 contains three non-inverting signal converters which can be used to interface the positive logic levels or pulses (of duration greater than 100 nsec) of K and M series to DIGITAL negative logic levels of −3 volts and ground. These converters provide current drive at a low output impedance so that unterminated cables or wires can be driven with a minimum of ringing and reflections.

The converters operate at frequencies up to 2 Mc with maximum rise and fall total transition of respectively 75 nsec and 115 nsec. By grounding pin E2 (L2 or R2) the rise and fall total transition times can be increased to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 500 KHz with typical rise and fall total transition times of 500 nsec.

A positive AND condition at the input gate produces a ground output. If any input is at ground the converter output is at −3 volts.

**Inputs:** Each input presents 1 unit load.

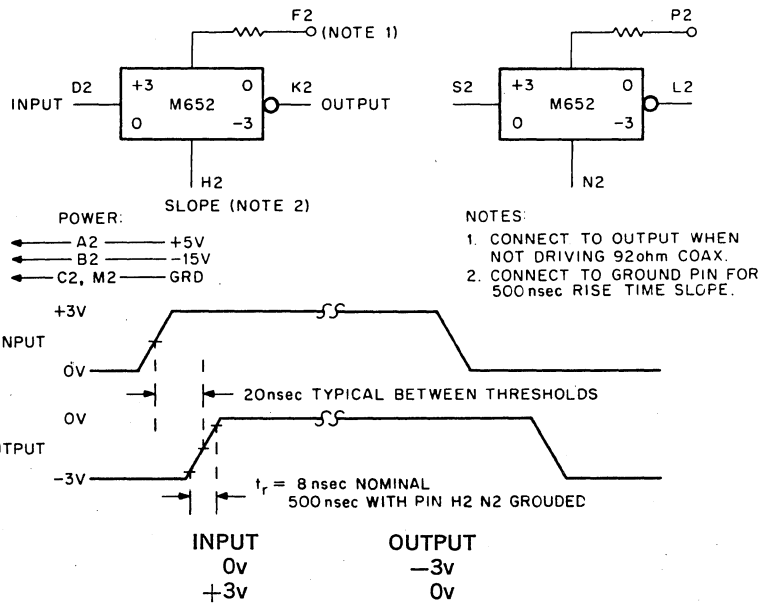
**Outputs:** Each output is capable of driving 20 ma. at ground and at −3 volts.

**Power:** +5 volts, 37 ma. (max.); −15 volts, 29 ma. (max.)

M650 — $25

# NEGATIVE OUTPUT CONVERTER
## M652

**M SERIES**




| INPUT | OUTPUT |
|---|---|
| 0v | −3v |
| +3v | 0v |

The M652 contains two non-inverting high-speed signal converters which can be used to interface the positive logic levels or pulses of the K and M Series to DIGITAL negative logic levels of −3 volts and ground. These converters provide current drive at a low output impedance so that system interconnections can be made using terminated 92-ohm coaxial cable. The conerters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec. The slope of the output transition can be decreased by grounding an internal RC network, to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 1 MHz.

**Inputs:** Positive logic levels of 0 and +3 volts (nominal). Input loading is 2 unit loads. Input signals more positive than +6 volts will damage the circuit.

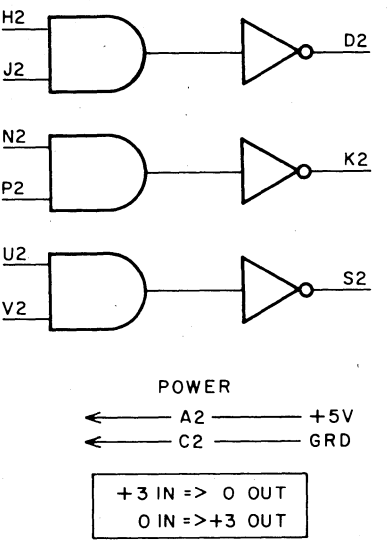
**Outputs:** Each output can drive terminated 92 ohm coaxial cable and supply an additional 20 ma. at ground or sink an additional 20 ma. at −3 volts. Output rise and fall times are dependent on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds will be increased by connecting the 100-ohm resistor to the output.

**Power:** +5 volts, 122 ma. (max.); −15 volts, 202 ma. (max.)

M652 — $26

# POSITIVE LEVEL DRIVER
## M660

**M SERIES**




The M660 Cable Driver consists of three circuits each of which will drive 100 ohm terminated cable with M Series levels or pulses whose duration is greater than 100 nsec.

**Inputs:** Each input represents 1 unit load.

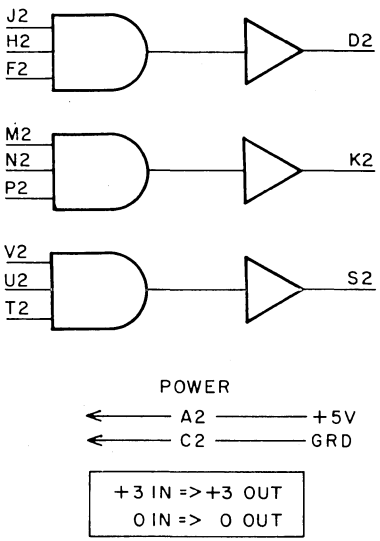
**Outputs:** M Series logic levels with 50 ma. drive current at logic "1" or "0".

**Power:** +5v, 71 ma. (max.)

M660 — $25

# POSITIVE LEVEL DRIVER
M661

**M SERIES**




The M661 contains three circuits which may be used to drive low impedance unterminated cable with M Series logic levels or pulses whose duration is 100 nsec or greater.

**Inputs:** Each input represents 1 unit load.

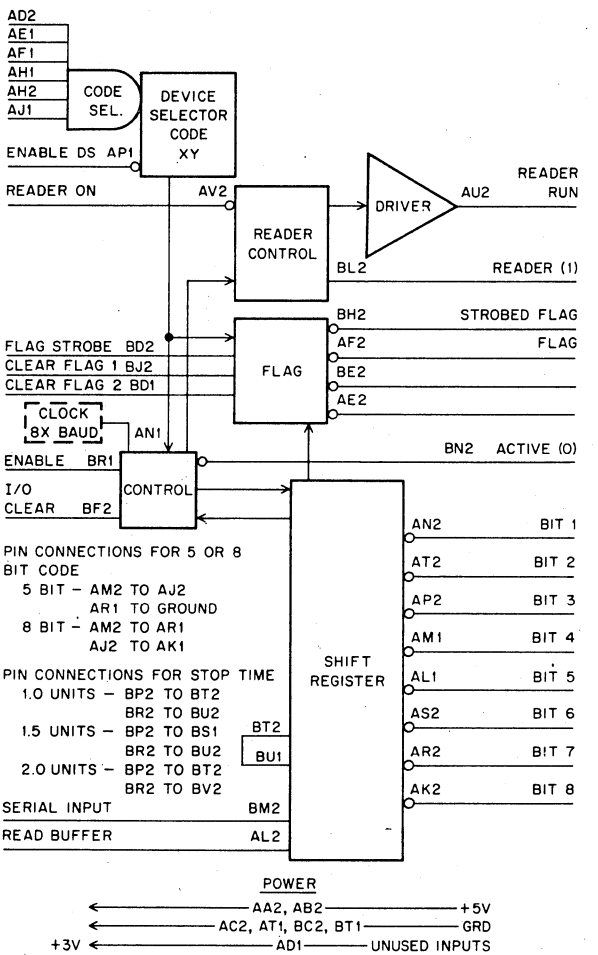
**Outputs:** M Series logic "1" at 5 ma.
M Series logic "0" at 20 ma.

**Power:** +5v, 111 ma. (max.)

M661 — $15

# TELETYPE RECEIVER
## M706

**M SERIES**



The M706 Teletype Receiver is a serial-to-parallel teletype code converter self contained on a double height module. This module includes all of the serial-to-parallel conversion, buffering, gating, and timing (excluding only an external clock necessary to transfer information in an asynchronous manner between a serial data line or teletype device and a parallel binary device). Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the M706 through the use of different pin connections on the module. When conversion is complete, the start and stop bits accompanying the serial character are removed. The serial character is expected to be received with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with reception of the center of bit eight, the Flag output goes low indicating that a new character is ready for transmission into the parallel device. The parallel data is available at the Bit 1 through Bit 8 outputs until the beginning of the start bit of a new serial character as received on the serial input. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M706 includes the necessary logic to provide rejection of spurious start bits less than one-half unit long, and half-duplex system operation in conjunction with the M707. Device selector gating is also provided so that this module can be used on the positive I/O bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M706, write for Applications Note AP-M-013.

**Inputs:** All inputs present one TTL unit load except where noted. When input pulses are required, they must have a width of 50 nsec or greater.

**Clock:** The clock frequency must be eight times the serial input bit rate (baud rate). This input can be either pulses or a square wave. Input loading on the clock line is three unit loads.

**Enable:** This input when brought to ground will inhibit reception of new characters. It can be grounded any time during character reception, but returned high only between the time the Flag output goes to ground and a new character start bit is received at the serial input. When not used this input should be tied to a source of +3 volts.

**I/O Clear:** A high level or positive pulse at this input clears the Flag and initializes the state of the control. When not used, or during reception, this input should be at ground.

**Code Select Inputs:** When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Read Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex receiver modules when a signal like Read Buffer is common to many modules. The inputs can also be used for device Selector inputs when the M706 is used on the positive I/O bus of the PDP8/I or PDP8/L. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to bypass the code select inputs, they can be left open and the Enable D.S. line tied to ground.

**Clear Flag 1:** A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared is a maximum of 100 nsec. The Flag cannot be set if this input is held high.

**Clear Flag 2:** A high level or positive pulse at this input, independent of the state of the code select inputs, will clear the Flag. All other characteristics are identical to those of Clear Flag 1.

**Flag Strobe:** If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

**Read Buffer:** A high level or positive pulse at this input while the code select inputs are all high will transfer the state of the shift register to outputs Bit 1 through Bit 8. Final parallel character data can be read by this input as soon as the Flag output goes to ground. Output data will be available a maximum of 100 nsec after the rising edge of this input. See the timing diagram of Figure 1 for additional information.

**Reader On:** A low level or ground at this input will turn the internal reader flip-flop on. This element is turned off at the beginning of a received character start bit. This input can also be pulsed by tying it to one of the signals derived at output pins AE2 or BE2. A low output will exist at pin BE2 if the M706 is addressed and the clear Flag 1 (pin BJ2) is high. A low output will exist at pin AE2 if the M706 is addressed and the Clear Flag 1 (pin BJ2) is high or if Clear Flag 2 (pin BD1) is high.

**Serial Input:** Serial data received on this input is expected to have a logical zero (space) equal to +3 volts and a logical 1 (mark) of ground. The input receiver on the M706 is a schmitt trigger with hysterisis thresholds of nominally 1.0 and 1.7 volts so that serial input data can be filtered up to 10% of bit width on each transition to remove noise. This input is diode protected from voltage overshoot above +5.9 volts and undershoot below —0.9 volts. Input loading is four unit loads.

**Outputs:** All outputs can drive ten unit loads unless otherwise specified.

**Bits 1 through 8:** A read Buffer input signal will transfer the present shift register contents to these outputs with a received logical 1 appearing as a ground output. If the Read Buffer input is not present, all outputs are at logical 1. When the M706 is used for reception of 5-bit character codes, the ouput data will appear on output lines Bit 1 through 5 and bits 6, 7, 8 will have received logical zeros.

**Active (0):** This output goes low at the beginning of the start bit of each received character and returns high at the completion of reception of bit 8 for an 8-bit character or of bit 5 for a 5-bit character. Since this signal uses from ground to +3 volts one-half bit time after the Flag output goes to ground, it can be used to clear the flag through Clear Flag 2 input while the Flag Output after being inverted can strobe parallel data out when connected to Read Buffer.

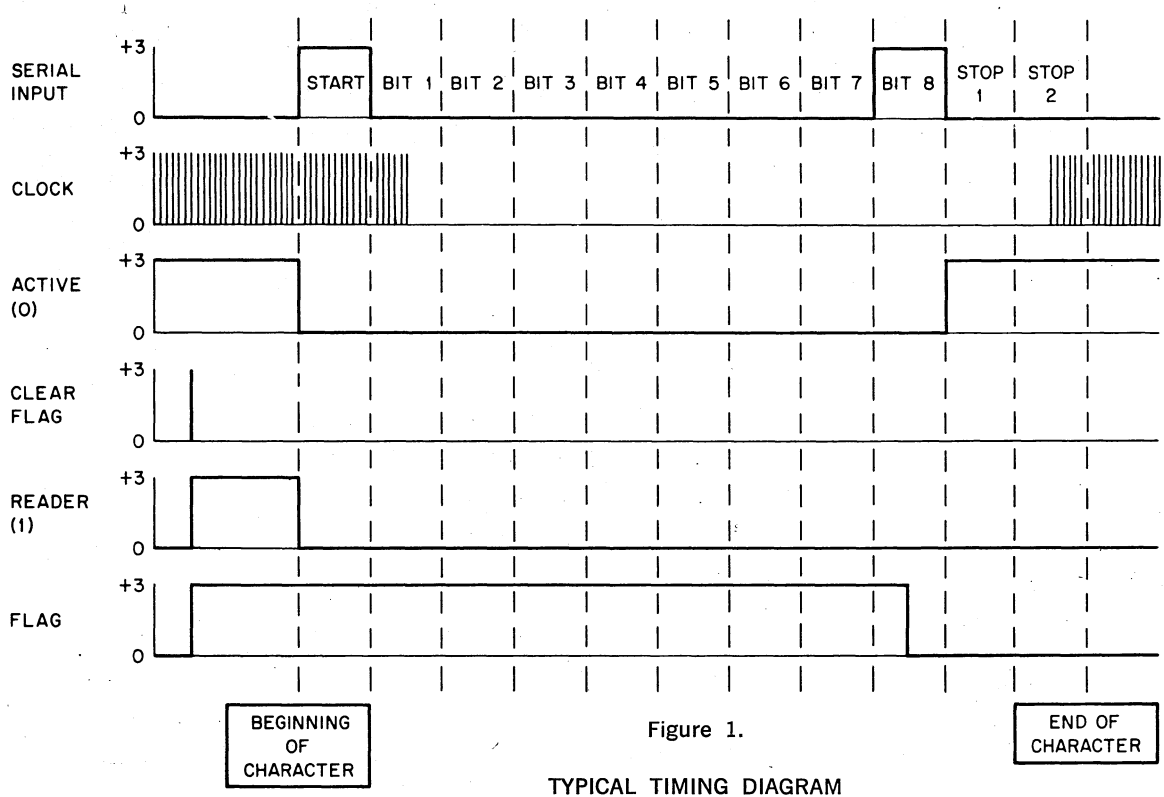



Figure 1.

TYPICAL TIMING DIAGRAM
Serial Input-Parallel Output 8-Bit (01, 111, 111)-2 Unit Stop Time

If an M706 and M707 are to be used in half duplex mode, this output should be tied to the Wait input of the M707 to inhibit M707 transmission during M706 reception. Output drive is eight unit loads.

**Flag:** This output falls from +3 volts to ground when the serial character data has been fully converted to parallel form. Relative to serial bit positions, this time occurs during the center of either bit 8 or bit 5 depending respectively on the character length. If the M706 is receiving at a maximum character rate, i.e. one character immediately follows another; the parallel output data is available for transfer from the time the Flag output falls to ground until the beginning of a new start bit. This is Stop bit time plus one-half bit time.

**Strobed Flag:** This output is the NAND realization of the inverted Flag output and Flag Strobe.

**Reader (1):** Whenever the internal reader flip-flop is set by the Reader ON input, this output rises to +3 volts. It is cleared whenever a start bit of a new character received on the serial input.

**Reader Run:** For use with Digital modified ASR33 and ASR35 teletypes which have relay controlled paper tape readers. This output can drive a 20 ma at +0.7 volts load. The common end of the load can be returned to any negative voltage not exceeding —20 volts.

**Pin AE2:** This output is the logical realization of NOT (Clear Flag 1 or Clear Flag 2 or I/O Clear) and is a +3 volts to ground output level or pulse depending on the input. This signal can be used to pulse Reader On for control of Reader Run as used in DEC PDP8/I or PDP8/L computers.

**Pin BE2:** This output is brought from +3 volts to ground by an enabled Clear Flag 1 input. It can be connected to Reader On for a different form of control of Reader Run.

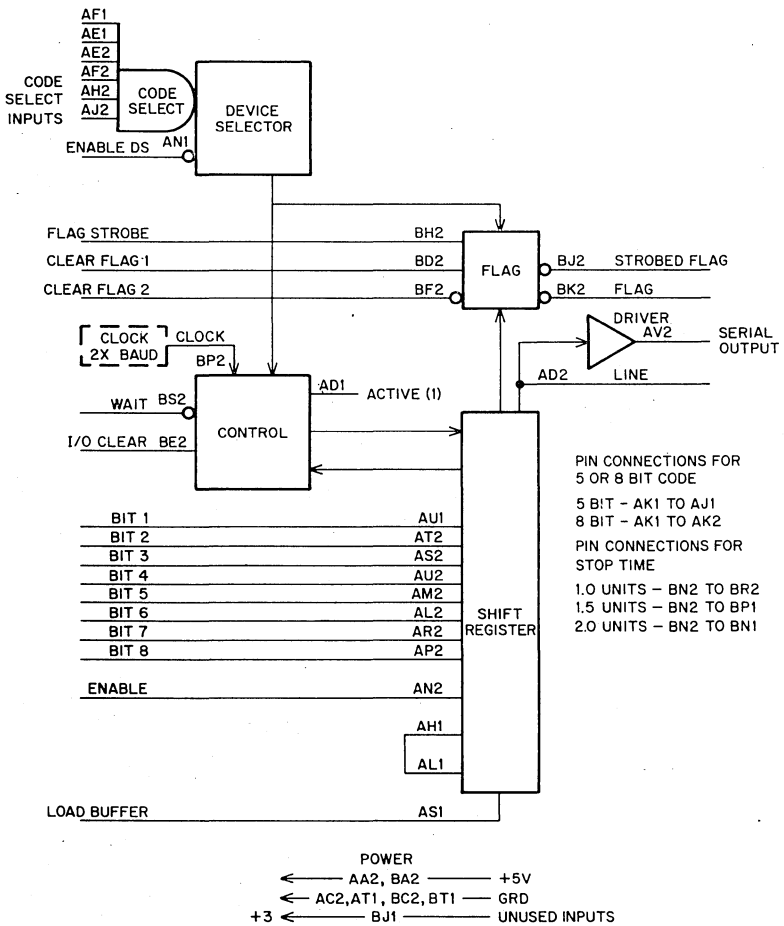
**+3 Volts:** Pin AD1 can drive ten unit loads at a +3 volt level.

**Power:** +5 volts at 400 ma. (max.).

M706 — $150

# TELETYPE TRANSMITTER
## M707

**M SERIES**



The M707 Teletype Transmitter is a parallel-to-serial teletype code converter self contained on a double height module. This module includes all of the parallel-to-serial conversion, buffering, gating, and timing (excluding only an external clock) necessary tot ransfer information in an asynchronous manner between a parallel binary device and a serial data line or teletype device. Either a 5-bit or an 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character or a 10.0, 10.5, or 11.0 unit serial character by the M707 through the use of different pin connections on the module. When conversion is complete, the necessary start bit and selected stop bits (1.0, 1.5, or 2.0 units) have been added to the original parallel character and transmitted over the serial line. The serial character is transmitted with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with the stop bit being put on the serial line, the Flag output goes low indicating that the previous character has been transmitted and a new parallel character can be loaded into the M707. Transmission of this new character will not occur until the stop bits from the previous character are completed. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M707 includes the necessary gating so that it can be used in a half-duplex system with the M706. Device selector gating is also provided so that this module can be used on the positive bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M707 write for Applications Note AP-M-013.

**Inputs:** All inputs present one TTL unit load with the exception of the Clock input which presents ten unit loads. Where the use of input pulses is required, they must have width of 50 nsec or greater.

**Clock:** The clock frequency must be twice the serial output bit rate. This input can be either pulses or a square wave.

**Bits 1 through 8:** A high level at these inputs is reflected as a logic 1 or mark in the serial output. When a 5-bit code is used, bit inputs 1 through 5 should contain the parallel data, bit 6 should be considered as an Enable, and bits 7, 8 and Enable should be grounded.

**Enable:** This input provides the control flexibility necessary for transmitter multiplexing. When grounded during a Load Buffer pulse, this input prevents transmission of a character. It can be driven from the output of an M161 for scanning purposes or in the case of a single transmitter, simply tied to +3 volts.

**Wait:** If this input is grounded prior to the stop bits of a transmitted character, it will hold transmission of a succeeding character until it is brought to a high level. A ground on this line will not prevent a new character from being loaded into the shift register. This line is normally connected to Active (0) on a M706 in half duplex two wire systems. When not used, this line should be tied to +3 volts.

**Code Select Inputs:** When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Load Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex transmitter modules when signals like Load Buffer are common to many modules. These inputs can also be used for device selector inputs when the M707 is used on the positive bus of the PDP8/I or PDP8/L. The

code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to by-pass the code select inputs, they can be left open and the Enable DS line tied to ground.

**Clear Flag 1:** A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared at the Flag output is a maximum of 100 nsec. The Flag cannot be set if this input is held at logic 1.

**Clear Flag 2:** A low level or negative pulse at this input will clear the Flag. When not used this input should be tied to +3 volts. The Flag will remain cleared if this input is grounded. Propagation from input fall to Flag output rise is a maximum of 80 nsec. If it is desired to clear the flag on a load buffer pulse, Clear Flag 2 can be tied to pin AR1 of the module.

**Flag Strobe:** If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

**I/O Clear:** A high level or positive pulse at this input clears the Flag, clears the shift register and initializes the state of the control. This signal is not necessary if the first serial character transmitted after power turn-on need not be correct. When not used, or during transmission, this input should be at ground.

**Load Buffer:** A high level or positive pulse at this input while the code select inputs are all high will load the shift register buffer with the character to be transmitted. If the Enable input is high when this input occurs, transmission will begin as soon as the stop bits from the previous character are counted out. If a level is used, it must be returned to ground within one bit time (twice the period of the clock).

**Outputs:** All outputs present TTL logic levels except the serial output driver which is an open collector PNP transistor with emitter returned to +5 volts.

**Serial Output:** This open collector PNP transistor output can drive 20 ma into any load returned to a voltage between +4 volts and −15 volts. A logical output or mark is +5 volts and a logical 0 or space is an open circuit. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a high speed silicon diode to the output and the diode anode to the coil supply voltage.

**Line:** This output can drive ten TTL unit loads and presents the serial output signal with a logical 1 as +3 volts and logical 0 as ground.

**Active:** During the time period from the occurrence of the serial start bit and the beginning of the stop bits, this output is high. This signal is often used in half duplex systems to obtain special control signals. Output drive is eight TTL unit loads.

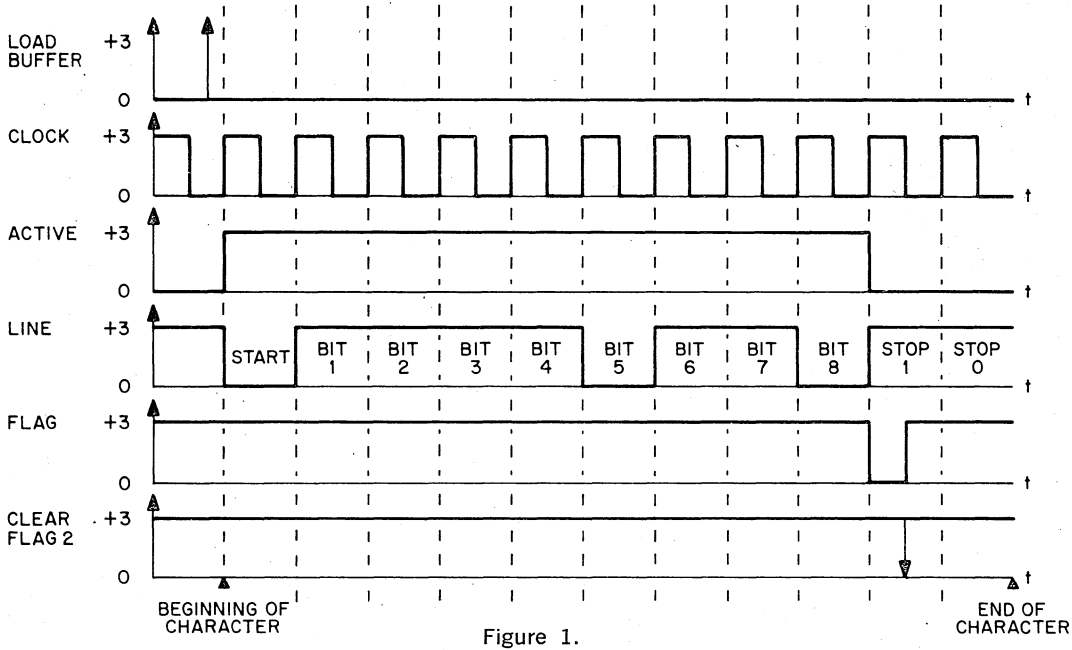



Figure 1.

Typical Timing Diagram, Parallel
input, 8-Bit Character (11, 110, 110) With two bit Stop time.

**Flag:** This output falls from +3 volts to ground at the beginning of the stop bits driving a character transmission. The M707 can now be reloaded and the Flag cleared (set to +3 volts). This output can drive ten TTL unit loads.

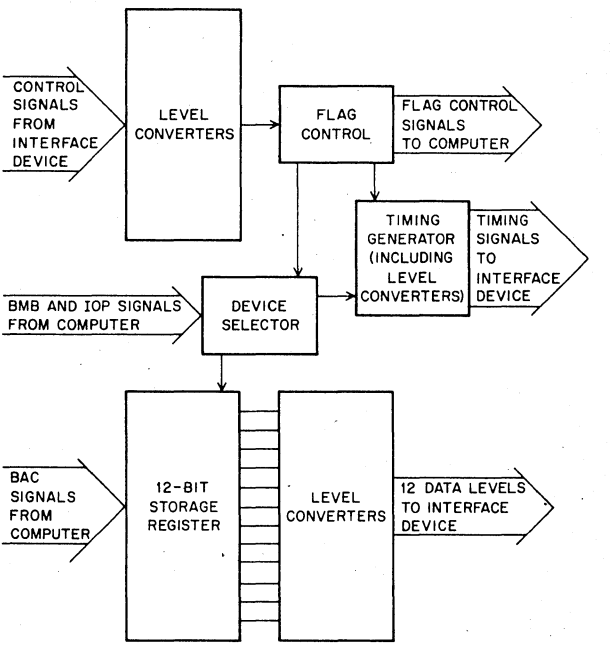
**Strobed Flag:** This output is the NAND realization of the inverted Flag output and Flag Strobe. Output drive is ten TTL unit loads.
+3 volts: Pin BJ1 can drive ten TTL unit loads at a +3 volt level.

**Power:** +5 volts at 375 ma. (max.)

M707 — $150

# BUS INTERFACE
## TYPES M730 & M731

**M SERIES**




The M730 and M731 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the output half of the programmed I/O transfer bus of either a PDP8/I or a PDP8/L positive bus computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to receive data from that computer, can to a large degree be interfaced by either the M730 or M731. Basic restrictions on the device or system to be interfaced are simply that it receive data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20 KHz. Complete interfaces to such peripheral gear as card punches and other repetitive devices is possible using the M730 and M731; however part of the controlling functions, such as counting etc. must be performed by computer software.

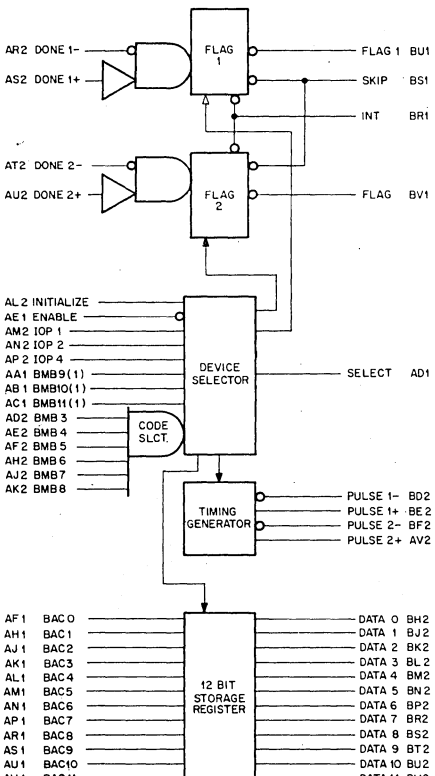



Figure 1

BUS INTERFACE — M730 (POSITIVE OUTPUT)

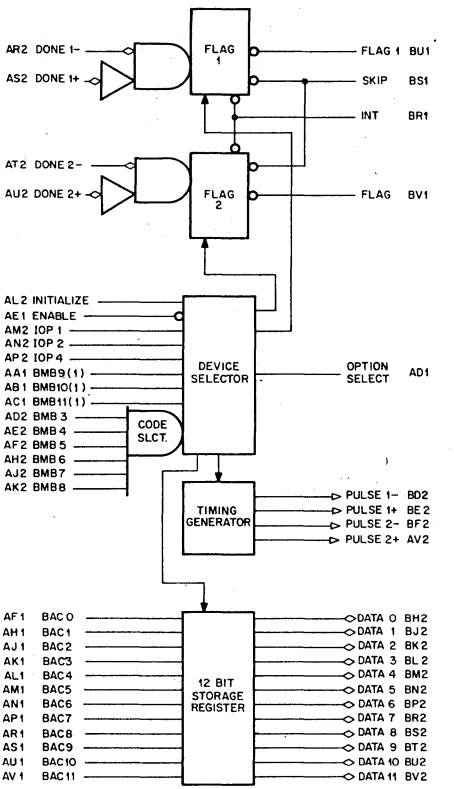



Figure 2

BUS INTERFACE — M731 (NEGATIVE OUTPUT)

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.

2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.

3. Storage Register—This 12-bit flip-flop buffer register provides output data storage for information to be transmitted to the interfaced device.

4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.

5. Level Converters—All level converters from the storage register or timing generator are open—collector transistor types which can drive 30 ma at ground. The M730 has npn drivers and can interface loads returned to a maximum positive supply of +20 volts and the M731 has pnp drivers which can interface loads returned to a maximum negative supply of −20 volts. Level converters which input control signals to the Flag control can receive signals of the same polarity and magnitude as the output drivers can sustain.

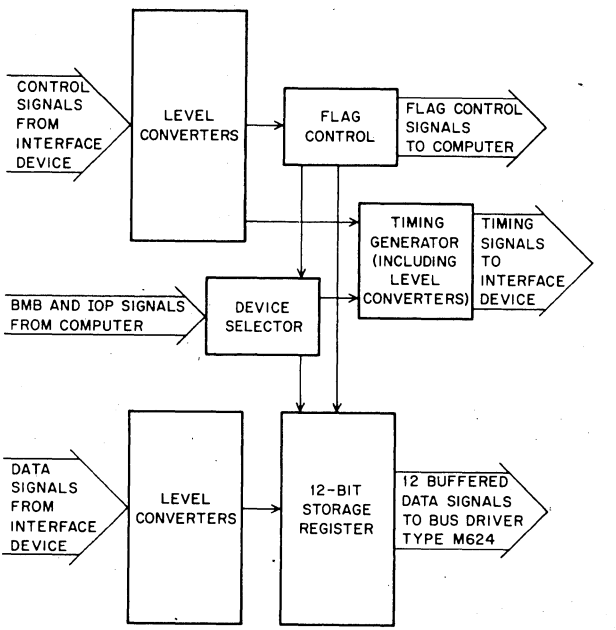
Thresholds on the input converters are +1.5 volts and −1.5 volts for the M730 and M731 respectively. All positive voltage levels are compatible with K and M series and all negative voltage signals are compatible with R, B and W Series.

For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales office. Application Note AP-M-017 contains useful information concerning the use of the M730 and M731.

M730 — $160
M731 — $160

# BUS INTERFACE
## TYPES M732 & M733

**M SERIES**




The M732 and M733 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the input half of the programmed I/O transfer bus of either a positive bus PDP8/I or PDP8/L computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to transmit data to that computer, can to a large degree be interfaced by either the M732 or M733. Basic restrictions on the device or system to be interfaced are simply that it transmit data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20KHZ. Complete interfaces to such peripheral gear as card readers and other repetitive devices is possible using the M732 and M733; however, part of the controlling functions such as counting, etc., must be performed by computer software.

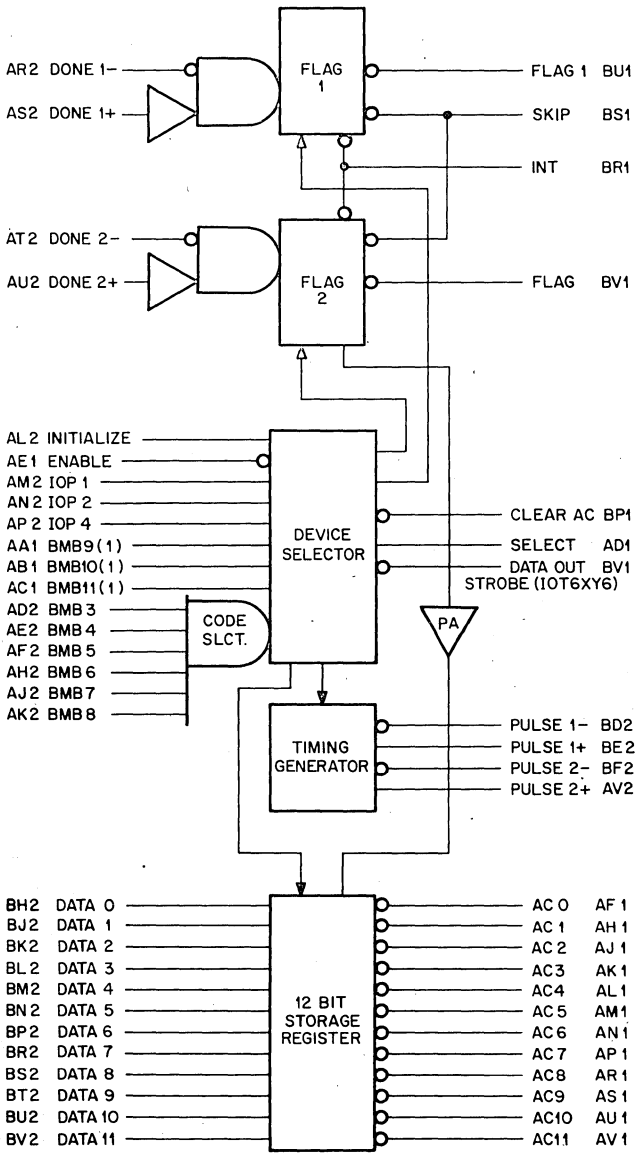



Figure 1

BUS INTERFACE — M732 (POSITIVE INPUT)

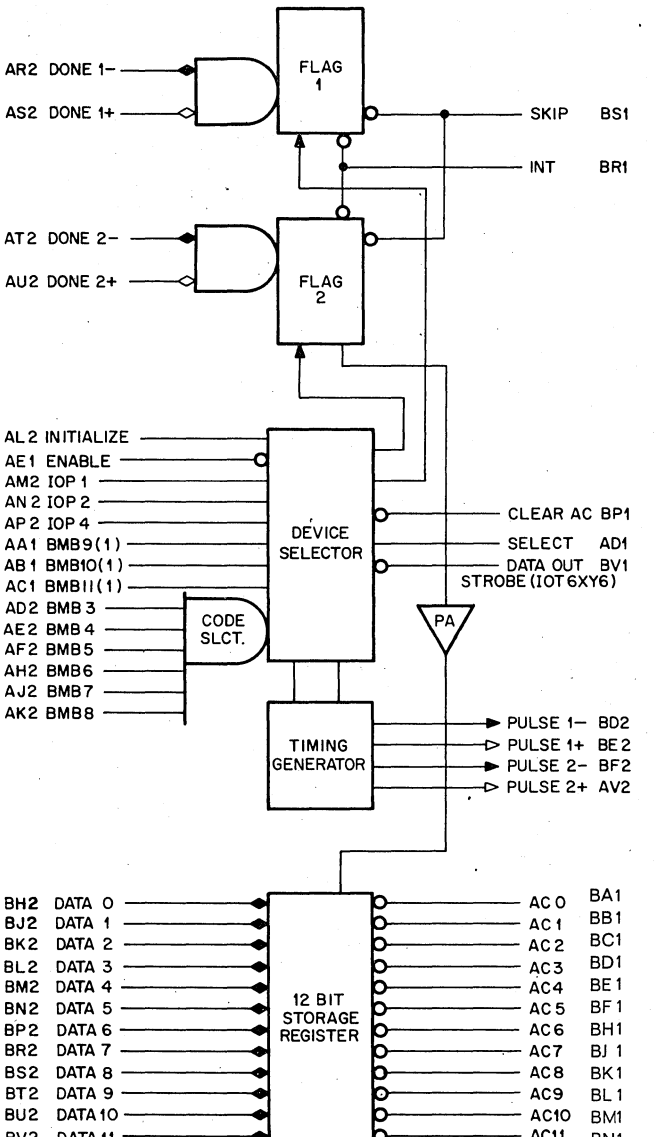



Figure 2

BUS INTERFACE — M733 (NEGATIVE INPUT)

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.

2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.

3. Storage Register—This 12-bit flip-flop buffer register provides input data storage of information received from the interfaced device. Information is loaded into this register by a control line from the peripheral.

4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.

5. Level Converters—All level converters from the timing generator are open collector transistor types which can drive 30 ma at ground. The M732 has npn drivers and can interface loads returned to a maximum positive supply of +20 volts and the M733 has pnp drivers which can interface to a maximum negative supply of −20 volts. Level converters which input control and data signals to these modules can receive signals of the same polarity and magnitude as the output drivers can sustain. Thresholds on the input converters are +1.5 volts and −1.5 volts for the M732 and M733 respectively.

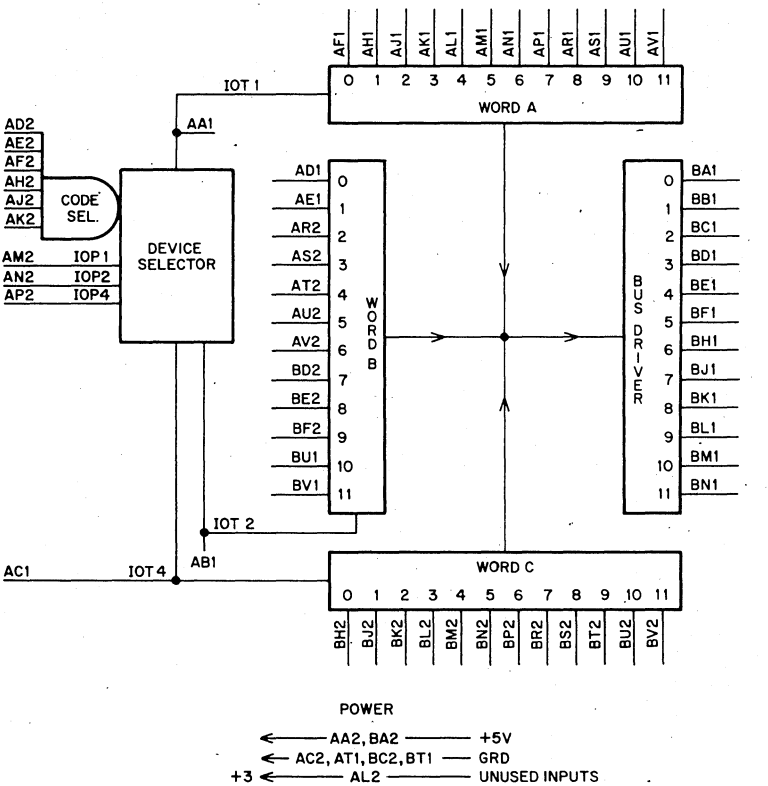
   All positive voltage levels are compatible with K and M Series and all voltage signals are compatible with R, B, and W Series.

For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales Office. Application Note AP-M-018 contains useful information concerning the use of the M732 and M733.

M732 — $160
M733 — $165

# I/O BUS INPUT MULTIPLEXER
## M734

**M SERIES**




The M734 is a double height, single width module and is a three word multiplexer used for strobing twelve-bit words on the positive voltage input bus; usually the input of the PDP8/I or the PDP8/L. Device selector gating is provided. The data outputs of the M734 Multiplexer consist of open collector npn transistors which allow these outputs to be directly connected to the bus. All inputs present one TTL unit load and function as follows:

Code select Inputs: When a positive AND condition occurs at these inputs, the pulse inputs IOP1, IOP2, and IOP4 are enabled for use in strobing input data. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts (Pin AL2). These inputs are all clamped so that no input can go more negative than —0.9 volts.

IOP1, 2, 4: These three 50 nsec or longer positive pulse inputs strobe respectively 12-bit words A, B, and C into the bus driver. All three lines are clamped so that no input can go more negative than —0.9 volts.

Data inputs: Bit 0-11 on words A, B, and C are strobed in 12-bit words as above. Bus driver output lines correspond numerically (0-11) to the selected word input lines (0-11). A high data input will force a bus driver output to ground during a data strobe. Inputs must be present at least 30 nsec prior to issuance of IOP 1, 2, or 4.

Bus driver: These open collector npn transistor bus driver outputs can sink 100 ma at ground. The maximum output voltage must not exceed +20 volts. Each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L, these outputs would be connected to the accumulator input lines of the I/O bus. Typical rise and fall TTT at these outputs with a 100 ma resistive load are 100 nsec.

Data Strobes: Pins AA1, AB1, and AC1 can each drive 18 TTL unit loads. These outputs appear coincident with IOP1, IOP2, and IOP4 respectively only if the code select inputs are all high.

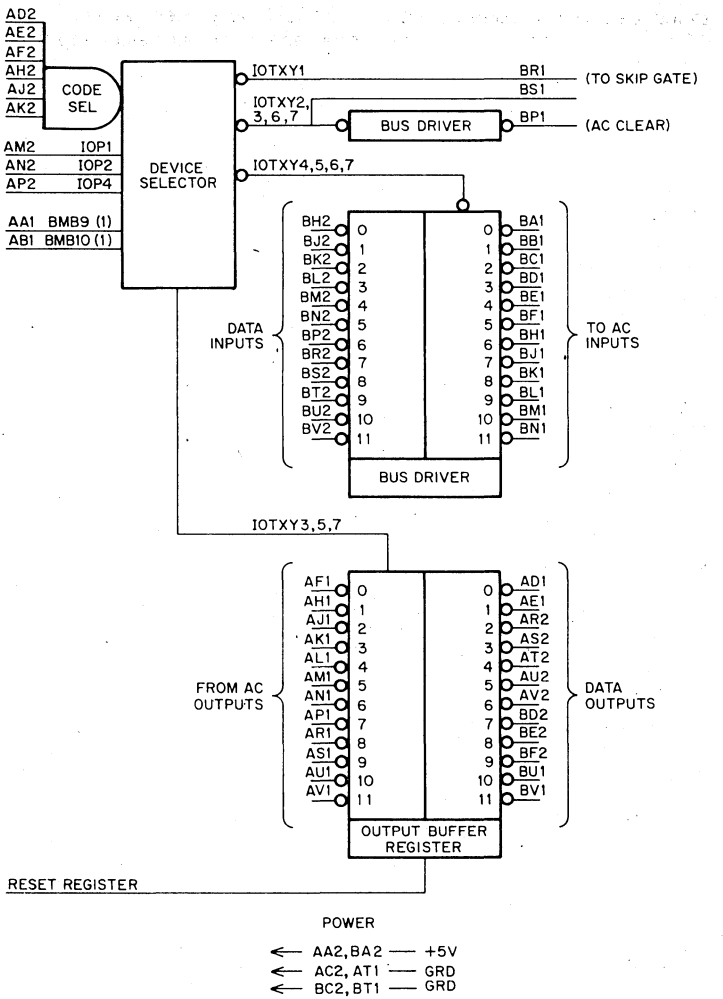
+3V — Pin AL2 can drive 19 inputs at a high logic level.

**Power:** +5 volts at 325 ma. (max.)

M734 — $105

# I/O BUS TRANSFER REGISTER
## M735

**M SERIES**




The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a complete interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.

**Inputs:**
All inputs present one TTL unit load with few exceptions as noted in the functional descriptions below:

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse input gates for IOP1, IOP2, and IOP4 are enabled for use as detailed below. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts. These inputs are all clamped so that no input can go more negative than —0.9 volts. When this module is used with the PDP8/I or PDP8/L these inputs would be connected to BMB outputs 3-8 to generate a device code. Where required in discussions below, this 6-bit device code will be referred to as code XY.

IOP1, 2, 4, BMB9(1) and BMB10(1): These three IOP's 50 nsec or longer positive pulse inputs, in conjunction with control level inputs BMB9(1) (Pin AA) and BMB10(1) (Pin AB1) provide all of the necessary signals for operation of this module. Table 1 below indicates the recommended use of these pulses and levels. A"1" or "0" in this table indicates the presence or absence respectively of a pulse (an IOP) or the logic level at pins AA1 or AB1.

The M735 module operation as associated with the various mnemonic IOT codes is quite explicit with the exception of IOTXY5. This code (IOTXY5) would be used to load zeros into the M735 with IOTXY1 and then to load into the AC the data present at the data inputs of the bus driver when IOTXY4 occurs. In this particular operation the AC has been effectively cleared as the content of the AC was zero during IOTXY1 thereby allowing the transfer of data into the AC without the use of the AC clear command usually generated by IOT2.

| IOP 4 | IOP 2 | IOP 1 | BMB 9(1) | BMB 10(1) | PDP/8 Mnemonic | Module Operation |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | IOTXY1 | +3V → OV output pulse on pin BR1 used for skip function. |
| 0 | 1 | 0 | 0 | 1 | IOTXY2 | +3V → OV output pulse on pin BS1, bus driver output on BP1 pulsed to ground and is used for the AC clear function. |
| 0 | 1 | 1 | 0 | 1 | IOTXY3 | Load output register from accumulator outputs on IOP1 execute IOTXY2. |
| 1 | 0 | 0 | 1 | 0 | IOTXY4 | Data inputs strobed onto accumulator inputs. |
| 1 | 0 | 1 | 1 | 0 | IOTXY5 | Load output register on IOP1, Execute IOTXY4. |
| 1 | 1 | 0 | 1 | 1 | IOTXY6 | Execute IOTXY2, and IOTXY4. |
| 1 | 1 | 1 | 1 | 1 | IOTXY7 | Execute IOTXY3, and IOTXY4. |

Although it is not implicit from Table 1, BMB9(1) and BMB10(1) inputs are gated in a positive OR circuit, so that when the M735 is not used on a PDP8/I or PDP8/L I/O bus one of these inputs can be grounded and the other used for control. They must appear at least 50 nsec prior to an IOP pulse. If the M735 is used with one of the above computers, these inputs must be tied to the corresponding I/O bus lines. The input load on IOP1 is two TTL unit loads. All five inputs are clamped so that no input can go more negative than —0.9 volts.

Data Inputs: Each data input when at ground, enables the corresponding bus driver output to be pulsed to ground during IOTXY4. A high input will inhibit the bus driver from being strobed. Since each input is ANDed with IOTXY4, any change of data after this strobe begins will change the bus driver output.

Accumulator Inputs: The input level presented to these inputs will be the same as that assumed by the buffer outputs after executing inputs strobes IOTXY , 5, or 7. Input data must be present at least 50 nsec prior to an IOP. Each input is protected from negative undershoot by a diode clamp.

Reset Register Pin AL2: A positive pulse of 50 nsec or longer at this input sets all buffer outputs to ground. When high, this input overrides any data loading from the accumulator inputs. The output register will be cleared within 70 nsec from the rising edge of this input. Diode input clamping is provided to limit negative undershoot to —0.9 volts.

**Outputs:**
Pin BR1: This output can drive ten TTL unit loads and has a propogation delay of less than 20 nsec. See Table 1.

Bus Driver: These open collector npn transistor bus driver outputs, including pin BP1, can sink 100 ma. at ground. The maximum output voltage cannot exceed +20 volts and each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L, output pins BA1—BN1 would be connected to the accumulator input lines and pin BP1 to the clear accumulator line of the I/O bus. Typical rise and fall TTT of these outputs with a 100 ma. resistive load are 100 nsec.

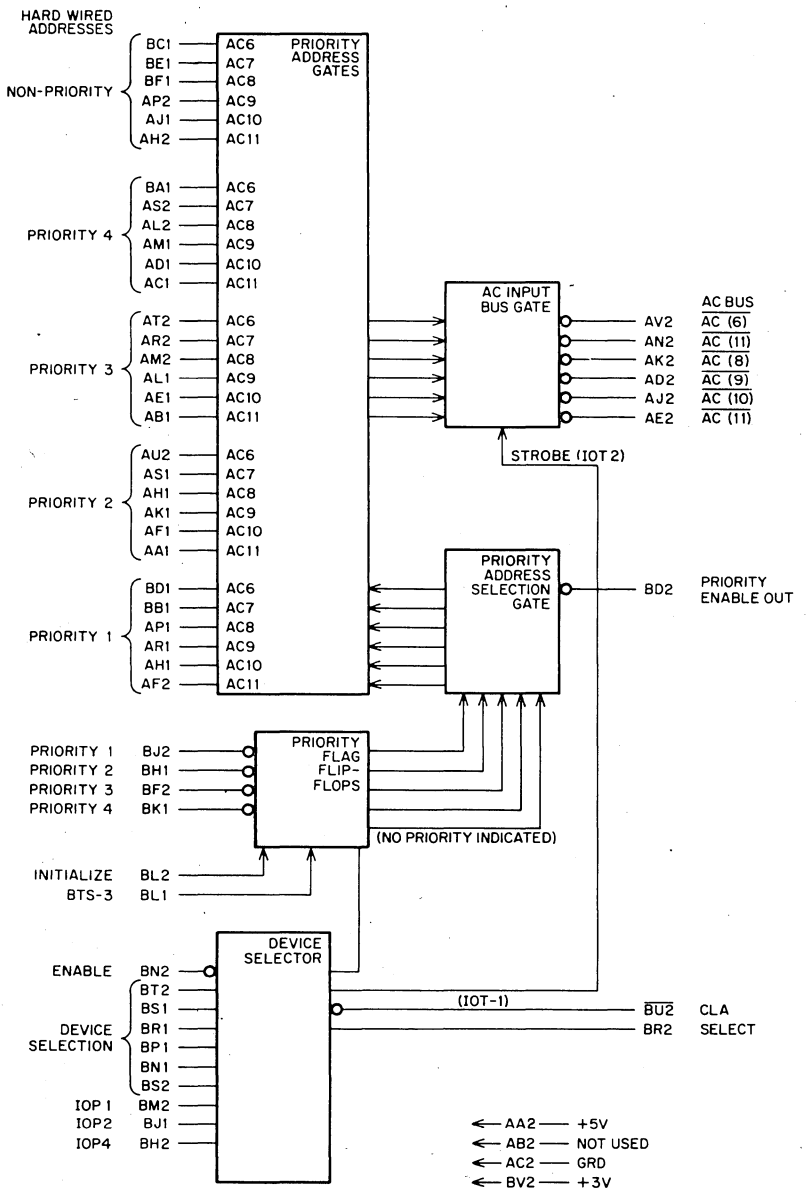
Buffer Outputs: Each output can drive ten TTL unit loads.

**Power:** +5 volts at 425 ma. (max.)

M735 — $135

# PRIORITY INTERRUPT MODULE
M736

M SERIES



# PRIORITY INTERRUPT MODULE
## M736

**M SERIES**

The M736 is used in conjunction with the PDP8/I or 8/L to provide the capability of assigning priorities to various I/O devices connected to the I/O bus of the computer. The M736 can be used to assign priorities for one thru four external devices. Priority assignment may be provided for more than four devices by using additional M736 modules for each additional group of four devices. All M736's in a particular priority system would utilize the same device code.

### THEORY OF OPERATION

Basically the M736 module consists of the following:

1. The M103 device selector function.
2. A Bit Time State-3 (BTS-3) input.
3. Four priority input lines.
4. Priority enable line, input and output.
5. Five groups of six gates, each of which is capable of being hard wired to provide address information to locate subroutings to service the various devices associated with the priority interrupt system. The output of each of these gates is strobed onto the accumulator input bus on lines AC(6) thru AC(11).

### SEQUENCE OF OPERATION

The external device activates its skip and/or interrupt FLAG flip-flop. The activation of the FLAG causes two things to happen; (a) The computer's interrupt request line is pulled to ground. This tells the computer that an external devices requires service and requests the computer to jump to an I/O priority interrupt service subroutine as soon as the computer completes its present cycle. (b) The external device FLAG pulls to ground the appropriate hard wired priority line connected to a "D" flip-flop in the M736.

A Bit Time State-3 (BTS-3) pulse from the computer is applied to the clock input of the "D" flip-flop to which the activating device flag is connected, as mentioned in section 1b above, and causes this flip-flop in the M736 to set. If more than one priority devices called to be serviced at the same time, all of the associated priority "D" flip-flops in the M736 would be set at this time. The outputs of the priority flip-flops in the M736 are connected to a priority gate structure which is arranged in such a manner that only one output line will be activated and that line will be associated with the external device with the highest priority.

This activated output of the priority gate structure is applied to one group of six two-input gates which make up the address gate. The other input of each of the six two-input gates of the address gate is hard wired to provide a discrete address which will correspond to the starting location of the particular

subroutine associated with that priority request. Each of the six output lines of the activated address gates is applied to one input of a two-input gate of the AC input strobe gate.

The computer now has had time to jump to the priority interrupt service routine and now issues a device selection code corresponding to the hard wired device selection code assigned to the M736 priority interrupt modules. This device selection code will pre-enable the IOP gates of the M736 of M736's.

The computer now issues an IOP-1 pulse to the IOP-1 gate of the M736 module. The output of the IOP-1 gate now produces an IOT-1 pulse which causes the "Clear the AC" line of the I/O bus to be pulled to ground, and thereby clears the AC.

The computer issues an IOP-2 pulse to the IOP-2 gate of the M736 module. The output of the IOP-2 gate produces an IOT-2 pulse which is applied to the strobe inputs of the AC input bus gate. As the other inputs of the AC input bus gate are connected to the outputs of the address gate, appropriate lines of the AC input bus (AC 6 thru AC 11) will be pulled to ground thereby loading into the AC the starting address of the subroutine associated with the particular priority I/O device to be serviced.

The computer now refuses to accept any further interrupt requests and jumps to the subroutine with the particular starting address which was loaded into the AC. The service routine of the particular priority device contains an instruction to clear the interrupt flag flip-flop of the particular I/O device and at the end of the subroutine issues the M736 device selector code with an IOP-4 which clears the priority flag flip-flops of the M736. The computer now turns on the priority interrupt system capability which allows the computer to service any future interrupt requests.

## USING THE M736 PRIORITY INTERRUPT MODULES

1. Assign a device selection code to the M736 priority system and connect the device selection inputs of the M736 to the proper device selection lines to assure decoding for that code. If more than one M736 is used connect the device selection lines for each M736 in exactly the same manner. Each M736 will use the same device selection code.
   These inputs are: BT2, BS1, BR1, BP1, BN1 and BS2.
2. Connect the enable input, BN2, of each M736 to GRD.
3. Connect the IOP-1 input, BM2, to the IOP-1 bus line.
4. Connect the IOP-2 input, BJ1, to the IOP-2 bus line.
5. Connect the IOP-4 input, BL2, to the IOP-4 bus line.
6. Connect the BTS-3 input, BL1, to the BTS-3 bus line.
7. Connect the outputs of the external I/O device flag flip-flops to the priority

NOTE: In normal operation, IOP-4, is not required as the flag flip-flop in the external priority I/O device is cleared by the subroutine servicing that device. When the flag in the I/O device is cleared, the next BTSO3 pulse will load the disabled flag outpu tinto its respective priority flag flip-flop in the M736 effectively clearing the priority flag flip-flop. flip-flop.

inputs in such a manner as to pull the corresponding priority input line of the M736 to GRD when the device flag is activated. These inputs are as follows:

| | | | |
|---|---|---|---|
| 1st priority | BJ2 | 1st | M736 Module |
| 2nd priority | BH1 | " | " " |
| 3rd priority | BF2 | " | " " |
| 4th priority | BK1 | " | " " |
| 5th priority | BJ2 | 2nd | " " |
| 6th priority | BH1 | " | " " |

Carry on for additional priority interrupt devices.

8. Assign starting address to the subroutines which will service each priority interrupt device attached to the priority interrupt system. Also assign a starting address for the subroutine to service non-priority devices. Hard-wire the various starting address of the service routines as follows:

| | AC(6) | AC(7) | AC(8) | AC(9) | AC(10) | AC(11) |
|---|---|---|---|---|---|---|
| Priority 1 | BD1 | BB1 | AP1 | AR1 | AH1 | AF2 |
| Priority 2 | AU2 | AS1 | AN1 | AK1 | AF1 | AA1 |
| Priority 3 | AT2 | AR2 | AM2 | AL2 | AE1 | AB1 |
| Priority 4 | BA1 | AS2 | AL2 | AM1 | AD1 | AC1 |
| NON-Priority | BC1 | BE1 | BF1 | AP2 | AJ1 | AH2 |

NOTE: If more than four external I/O devices require priority assignments, the NON-priority address inputs BC1, BE1, BF1, AP2, AJ1 and AH2 of the M736 module used for the first four highest priorities, *must* be connected to GRD. If more than two M736 modules are required all of the NON-priority address lines of each module except the last M736 containing the lowest priorities, must be connected to GRD. The NON-Priority address is hardwired to the NON-Priority address inputs of only the lowest priority M736 module. All un-used priority address inputs must be grounded. Logic 1 level for address may be obtained from module pin BV2 of each M736 module. Lower priority addresses would be hardwired on succeeding M736 modules in the same order hard wired to the second M736 module as follows:

| | AC(6) | AC(7) | AC(8) | AC(9) | AC(10) | AC(11) |
|---|---|---|---|---|---|---|
| Priority 5 | BD1 | BB1 | AP1 | AR1 | AH1 | AF2 |
| Priority 6 | AU2 | AH2 | AK2 | AD2 | AJ2 | AE2 |

9. Connect the AC input bus gate outputs to the AC bus as follows:

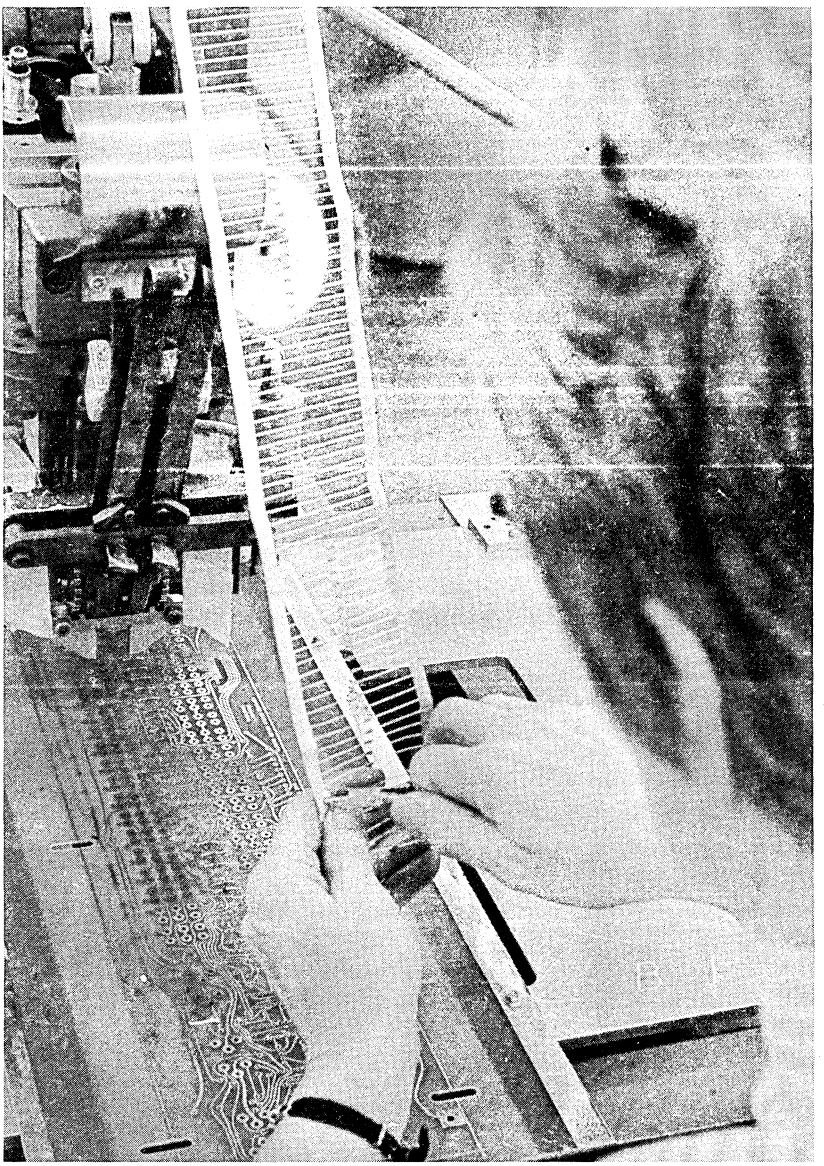
| | AC(6) | AC(7) | AC(8) | AC(9) | AC(10) | AC(11) |
|---|---|---|---|---|---|---|
| Module Pins | AV2 | AH2 | AK2 | AD2 | AJ2 | AE2 |

10. Connect the Priority Enable input line BE2, of the M736 with the highest priorities, or the only priorities, to ground.

11. If lower priorities of 5 or more are assigned, connect the Priority output of the module with the higher priorities, Pin BD2, to the next M736 module (with the next following four lesser priorities) Priority enable input pin BE2.

12. Last, but not least, connect the INITIALIZE input, BL2 to the Initialize line of the computer I/O bus.

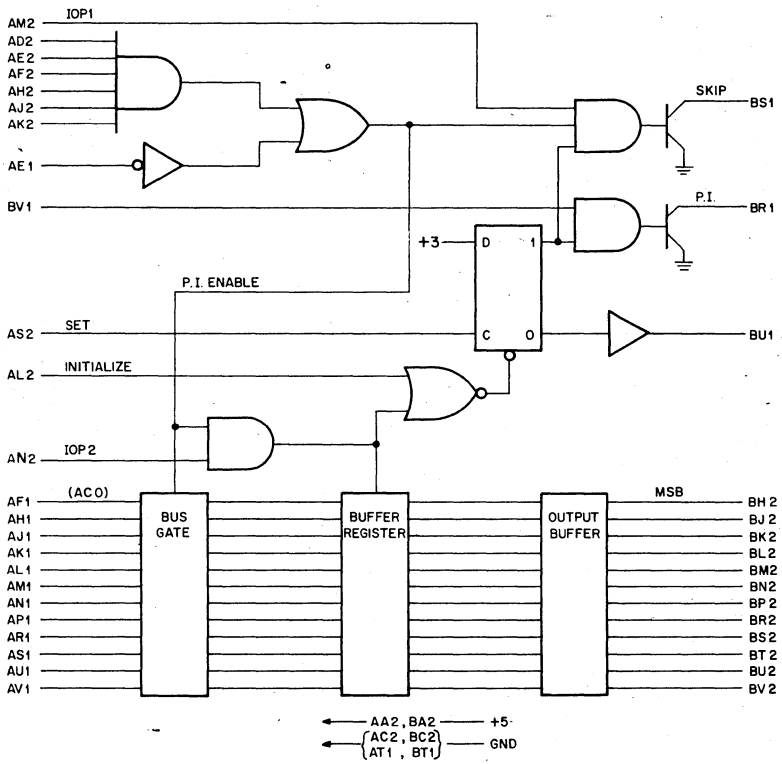
M736 — $125



These pantograph-controlled insertion machines position and crimp pre-tested components onto four module boards at a time. A press will cut the modules apart after assembly is completed, minimizing handling up to that point.

# 12-BIT BUS RECEIVER INTERFACE
## M737

**M SERIES**



The M737 12-Bit Bus Receiver Interface is completely contained on a double height, single width module.

The M737 was designed primarily to receive and store in a buffer register twelve parallel data bits from the positive bus of the PDP-8/I or PDP-8/L. The M737 is pin compatible with the M738 Counter-Buffer Interface, the M107 Device Selector, the M108 Flag Module, and the 12-Bit Bus Paneloid E100. The 12-Bit Bus Receiver Interface, M737, consists of three basic sections: device selector, flag, and buffer register section.

**Device Selector Section**
The device selector section contains six address inputs which are to be connected to the proper BMB bits for address selection. IOP 1 input is used to generate an IOT 1 which is used internally to test the flag. The output of flag test gate is connected directly to the skip bus with an NPN transistor. The output of the address selection gate is connected to the bus gate of the buffer register section and functions as an option select level. IOP 2 is used for two purposes. It is internally connected in such a manner as to clear the flag and to load the buffer register with the contents of the BAC lines.

**The Flag Section**
The flag section is used to generate a programmed interrupt. The flag flip-flop may be set by a level shift from low to high (a positive going voltage) applied to the set input at pin AS2. The output of the flag is connected to the P. I. line by way of a P. I. enable gate and an open collector NPN transistor. The output of the flag is also connected to pin BU1. The flag is reset by IOP2 applied to pin AN2 or by initialize pulses applied to Pin AL2.

**Buffer Register Section**
Data from the bus is applied to the inputs of the bus gate. The bus gate prevents the buffer register from loading the bus when M737 is not addressed. The bus gate is enabled by the option select level derived internally from the output of the device selector section. The buffer register is loaded by jam transfer upon the command of an IOT2 instruction. The output of the buffer register is buffered by the use of TTL circuitry.

**Inputs:** All inputs which receive positive bus signals are protected against negative voltage undershoot. AE1, BV1 represent 1.25 TTL unit loads. These two inputs need not be tied to a logic 1 source when not used.

AM2, AN2 represent 2.5 TTL unit loads.

AS2 represents 2 TTL unit loads.

All other inputs represent 1 TTL unit load.

**Outputs:** BS1, BR1 will sink 25 MA to ground. Voltage applied to these outputs must not be allowed to exceed +20 volts. These outputs are protected against negative voltage undershoot and consist of open collector NPN transistors.

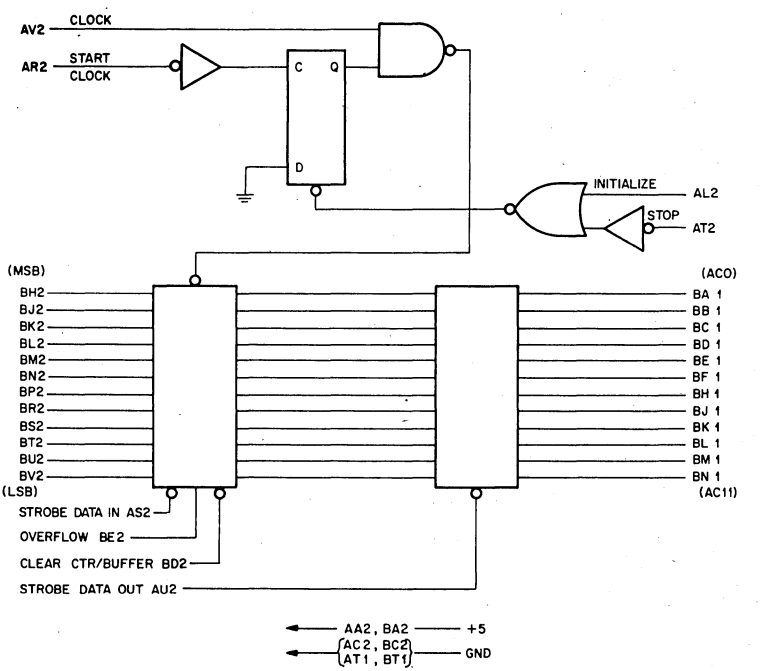
All other outputs will drive 10 TTL unit loads.

**Power:** +5 volts, 300 ma (maximum).

M737 — $120

# COUNTER-BUFFER INTERFACE
## M738

**M SERIES**




The M738 Counter-Buffer Interface is contained on a double height, single width module.

The M738 was designed primarily to strobe twelve parallel bits onto the positive bus of the PDP-8/I or PDP-8/L. This module consists of three basic sections: 1) A twelve bit bus driver, 2) A twelve bit Up Counter which is presetable by jam transfer, and 3) A clock input gate circuit twelve bit bus driver.

The twelve bit bus driver is used to strobe the contents of the buffer counter onto the bus when a logic 0 (gnd) is applied to the "Strobe Data Out" pin AU2. The output of the bus driver consists of an open collector NPN transistor which allows the data outputs of other M738 modules to be parallel in a collector OR to ground fashion.

These outputs can sink 225 MA to ground and are protected against negative voltage undershoot in excess of −.9v.

The input to the "Strobe Data Out" pin AU2 would normally be an IOT pulse derived from a M103 or M107.

**Twelve bit up counter-buffer:**
The twelve bit counter-buffer consists of three MSI, 4-bit presetable counters connected in tandem. Twelve parallel bits of data may be applied to the data inputs and then jam transferred into the counter by the application of a logical zero of time duration equal to or greater than 250 n seconds to the "Strobe Data In" pin AS2. This input could be an IOT pulse from a M102 or M107.

The contents of the counter may be cleared by the application of a logical zero of time duration equal to or greater than three micro-seconds applied to the "clear counter/buffer" input pin BD2. The requirement of a three micro-second pulse precludes the direct use of an IOT pulse for clearing the counter. If it is required to clear the counter by the command of an IOT pulse, a M302 dual delay multivibrator could be used to stretch the IOT pulse length. At times, it may be desirable to connect two or more M738 module counters in tandem. This may be accomplished by connecting the "overflow" output pin BE2 of the first M738 to the "clock" input pin AV2 of the next M738. The clear pulse time duration should be an additional 3 micro-seconds for each M738 added in tandem; i.e. 24 bits would require a 6 micro-second clear pulse.

**Clock Input Gate**
The clock input gate circuit contains a storage flip-flop which serves to gate a clock pulse applied to the "Clock" input, pin AV2, into the counter buffer. This flip-flop may be initialized by the application of a logic one pulse (+ voltage pulse) to pin AL2 or by a logic zero (ground pulse) applied to the "Stop" input AT2. When the flip-flop is initialized, clock pulses applied to the clock input, pin AV2, will *not* be counted. Clock pulses may be counted by setting the flip-flop with the application of a logic zero pulse to the "Start Clock" input AR2. The four inputs, clock, start clock, stop and initialize require a minimum pulse width of 50 nanoseconds and therefore could use IOT pulses derived from the device selectors M103 or M107.

**Inputs:**
AS2 3TTL Loads
AU2 12TTL Loads
All other inputs 1 TTL Load
(See text for timing considerations)

**Outputs:**
BE2 10TTL Loads

All other outputs consist of open collector NPN transistors which are capable of sinking 25 MA to ground. Voltage applied to these outputs must not exceed +20 volts. The outputs are diode protected against negative voltage undershoot in excess of −.9 volts.

**Power:**
+5v at 250 MA (maximum) — no strobe onto bus.
370 MA (maximum) — during bus strobe.

M738 — $105

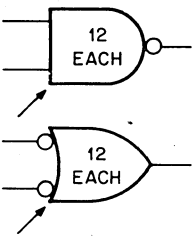
# LOGIC APPLIQUES

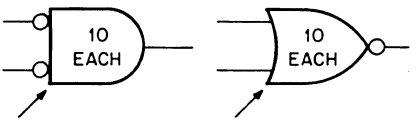
**M SERIES**

For convenient drawing of neat block diagrams, to supplement the DEC drawing template, self sticking matte-surface appliques lift from backing with a sharp knife.

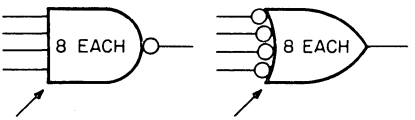
| DIAGRAMS | MODULES | APPLIQUE TYPE |
|---|---|---|
| 12 2-input NOR,<br>12 2-input NAND | M101, M113<br>K113, M141 | DRT-1-47 |
| 10 2-input NAND,<br>10 2-input NOR | M112 | DRT-1-03 |
| 8 4-input NOR,<br>8 4-input NAND | M117, M617,<br>M627 | DRT-1-35 |
| 10 8-input NOR,<br>10 8-input NAND | M119 | DRT-1-51 |
| 9 4-input AND/NOR<br>9 4-input NOR/AND | M121, M160 | DRT-1-25 |
| 3 Binary to Octal/Decimal Decoder | M161 | DRT-1-20 |
| 24 JK Flip-flops | M203, M206,<br>M207 | DRT-1-23 |
| 16 JK Flip-flops with gates | M204 | DRT-1-22 |
| 3 8-bit Buffer/Shift Register | M208 | DRT-1-41 |
| 18 Level Converters | M502, M652 | DRT-1-39 |
| 10 NOR Level Converters<br>10 NAND Level Converters | M506 | DRT-1-52 |
| 7 NOR Pulse Amplifiers<br>7 AND Pulse Amplifiers | M602, M650 | DRT-1-34 |
| 2 12-input AND/NOR<br>2 12-input NOR/AND<br>2 Timers, 2 clocks | M160, M302<br>M401 | DRT-1-21 |

PRICE: $1.50/sheet

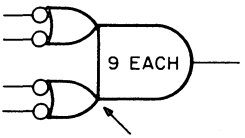


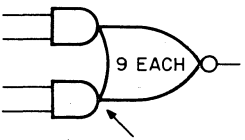




M117, M617, M627

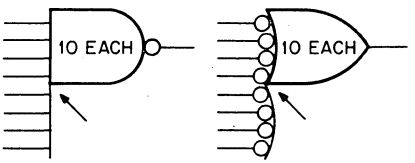



M121, M160

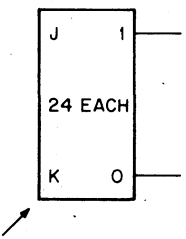


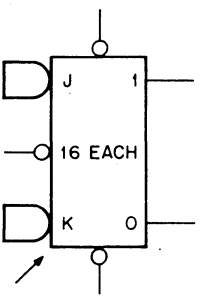

M119

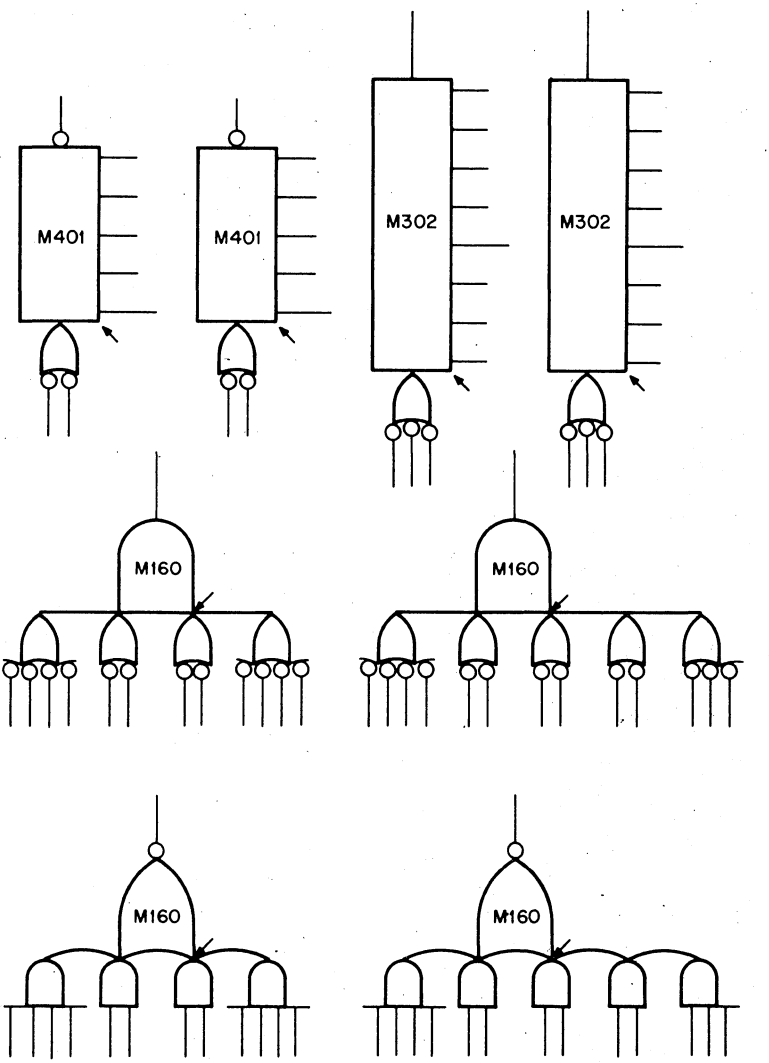



M203, M206, M207

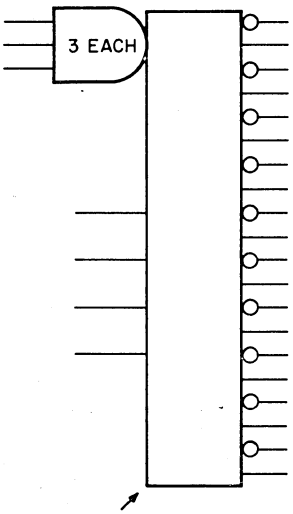



M204

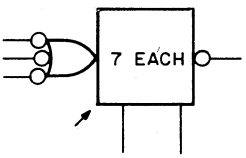


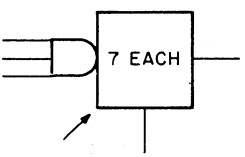

M401
M401
M302
M302
M160
M160
M160
M160

M161

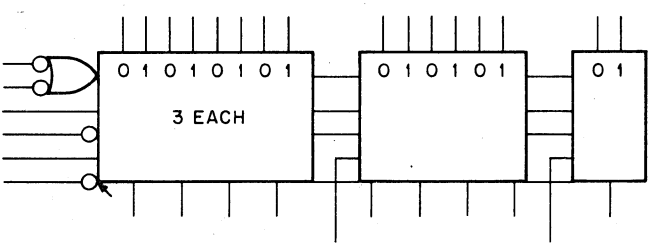



M602, M650

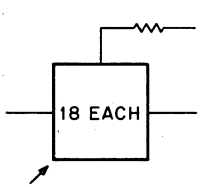


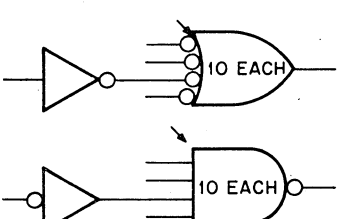

M208




M502, M652

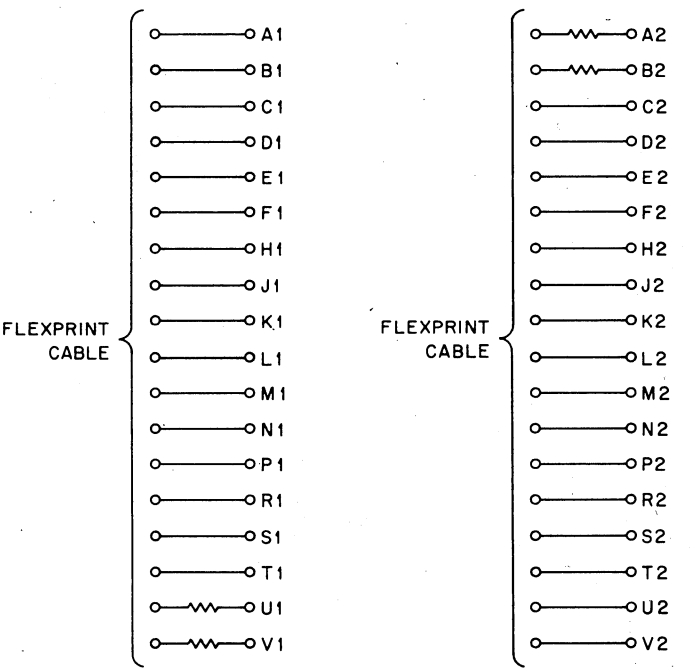



M506



# FLEXPRINT CABLE CONNECTOR
M901

**M SERIES**



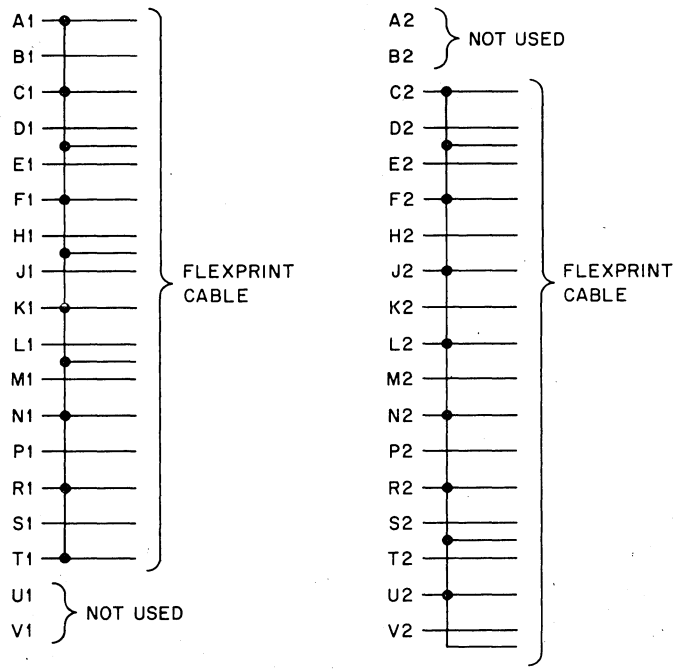

This module allows 36 lines to be used as signals and/or grounds. The 100 ohm resistors connected in series with the modules pins A2, B2, U1 and V1 are provided to afford some measure of protection in the event that these pins are inadvertently connected to a source of supply voltage.

**Input:** Recommended current per line is 100 ma. maximum.

M901 — $15

# FLEXPRINT CONNECTOR
M903

M SERIES




The M903 connector is a single sized, double sided board.

This connector provides high density cable connections using two single flexprint cables. Eighteen signal leads and grounds are used as listed below.

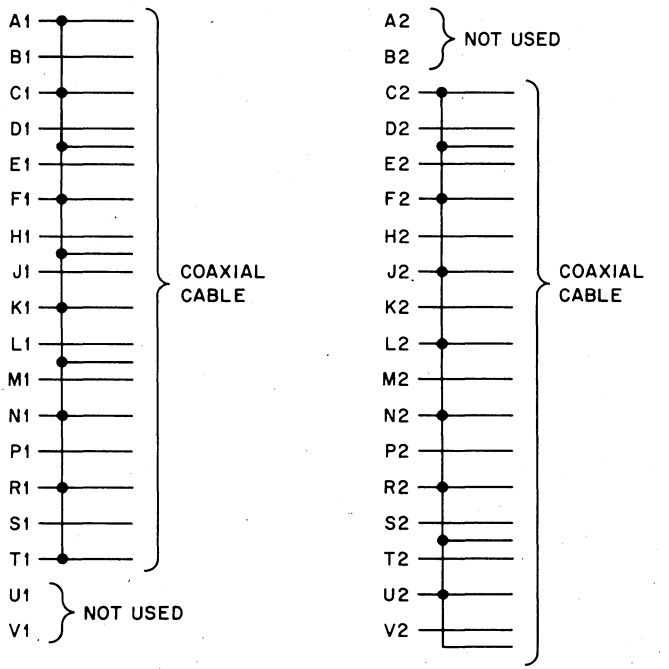
Signal: B1, D1, E1, H1, J1, L1, M1, P1, S1
D2, E2, H2, K2, M2, P2, S2, T2, V2

Common Ground: A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

M903 — $12

# COAXIAL CABLE CONNECTOR
M904

**M SERIES**




The M904 connector is a single sized, double sided board.

This connector provides high density cable connections using coaxial cable. Provisions are made for connection of two nine-conductor coaxial cables to this connector. Eighteen signal leads and grounds are used.

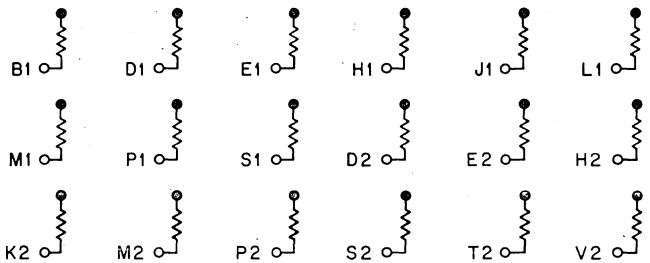
Signal: B1, D1, E1, H1, J1, L1, M1, P1, S1
D2, E2, H2, K2, M2, P2, S2, T2, V2

Common (ground): A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

M904 — $14

# CABLE TERMINATOR
## M906

**M SERIES**




The M906 cable terminator module contains 18 load resistors which are clamped to prevent excursions beyond +3V and ground. It may be used in conjunction with M623 to provide cable driving ability similar to M661 using fewer module slots.

The M906 may be used to terminate inputs. In this configuration, M906 and M111 are a good combination.

**Inputs:**
This module is normally used standard M-Series levels of 0 and +3V to partially terminate 100 ohm cable. It presents a load of 22.5 ma or 14 TTL unit loads at ground, and therefore, must be driven from at least an M617 type circuit, or preferably a cable driver.

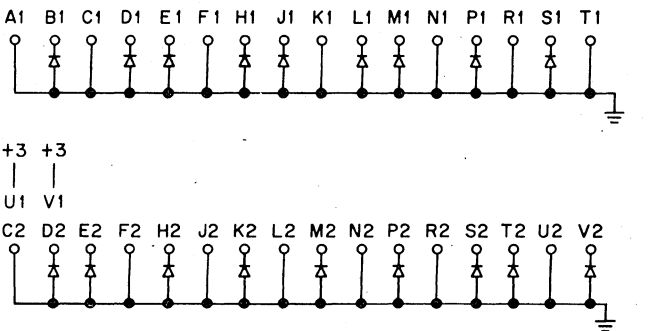
The following pins MUST be grounded: A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

**Power:** +5V @ 440 ma. (max.) (all lines grounded).

M906 — $20

# DIODE CLAMP CONNECTOR
M907

**M SERIES**




The M907 is used to provide proper undershoot ground clamps for PDP8/I positive bus signals not using M103 or M101 inputs.

The M907 also provides +3V for clamping 25 unused inputs. Diode clamps appear on signal leads used in double-sided alternate ground I/O cables.

Diode clamp: B1, D1, E1, H1, J1, L1, M1, P1, S1, D2, E2, H2, K2, M2, P2, S2, T2, V2

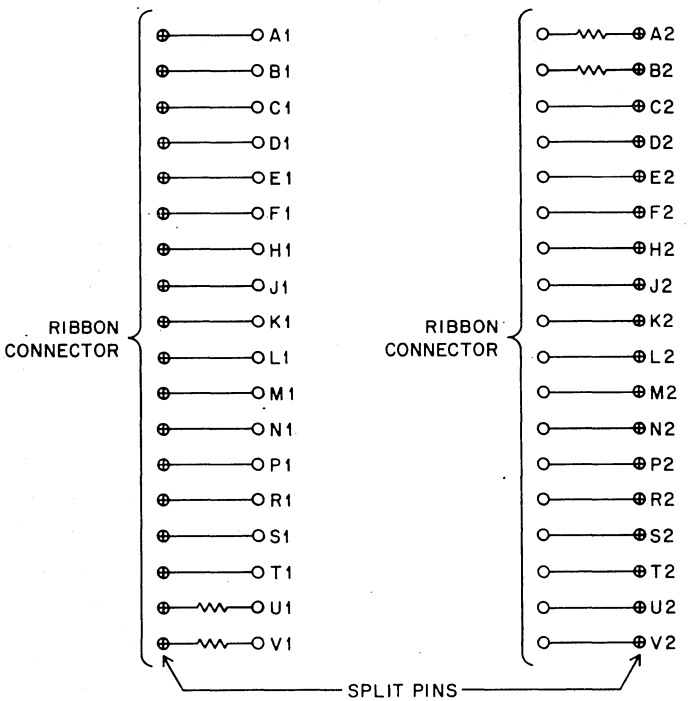
Ground: A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, U2

**Power:** +5v at 10.2 ma. (max.)

M907 — $16

# RIBBON CONNECTOR
## M908

**M SERIES**



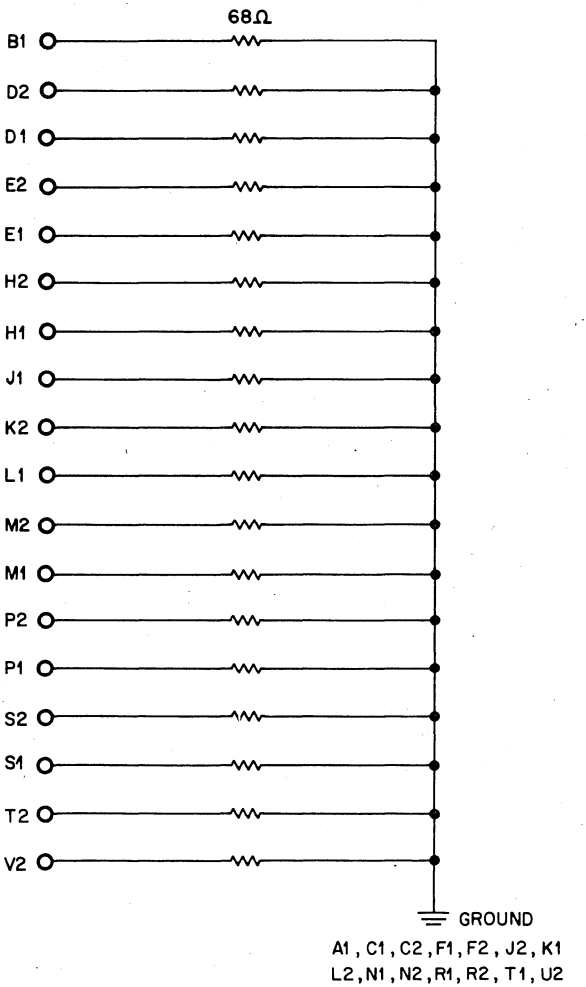

The M908 cable connector consists of a single sized, double sided board which contains thirty-six split pins which allows the connection of thirty-six separate wires. All connections are made on the component side of the module. The 10 ohm, ¼ watt resistors connected in series with module pins A2, B2, U1 and V1 are provided to afford some measure of protection in the event that these pins are inadvertently connected to a source of supply voltage.

The M908 is primarily intended for use with ribbon cable and is normally supplied with a ribbon cable clamp unless otherwise specified.

M908 — $18

# TERMINATION CARD
## M909

**M SERIES**



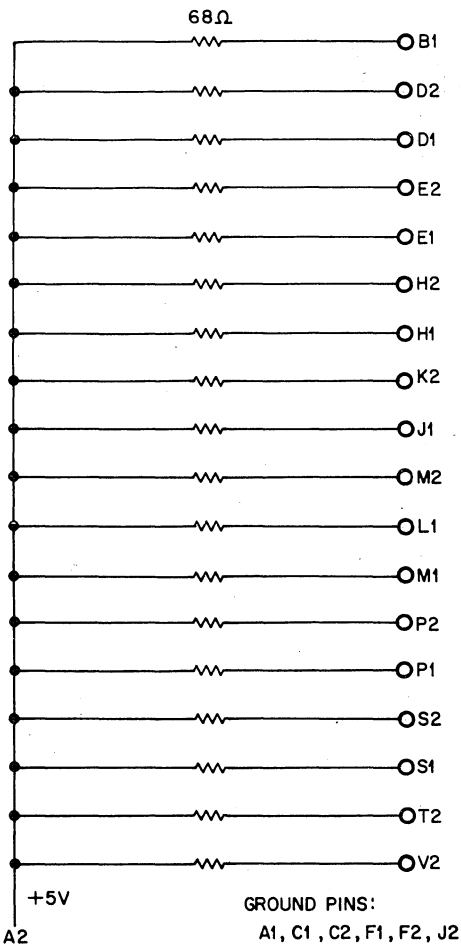

The M909 module contains 18 68Ω resistors. All 18 resistors are tied to ground through a common bus.

This module is used in conjunction with the M910 to form ½ of the biasing circuitry used in the driving network of the M622.

M909 — $14

# PULL UP RESISTOR
M910

M
SERIES



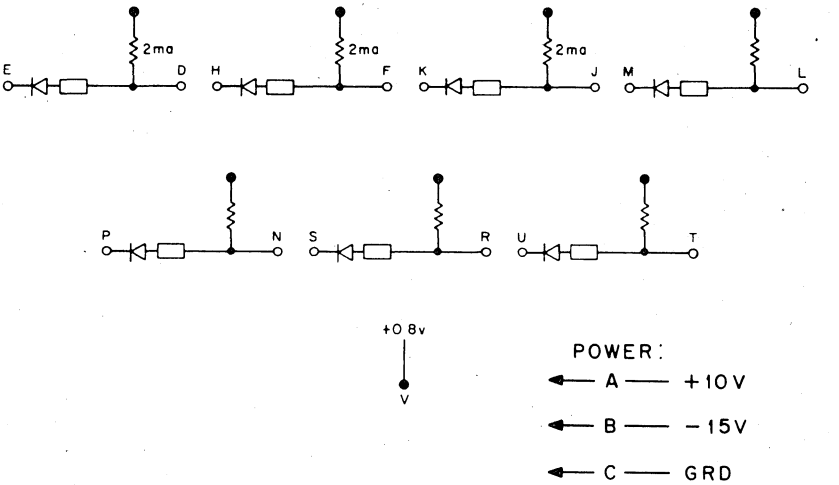

The M910 module contains 18-68Ω resistors. All resistors are tied to a common +5 volts bus.

This module is used in conjunction with the M909 to form ½ of the biasing circuitry used in the driving network of the M622.

M910 — $14

# POSITIVE LEVEL CONVERTER
W512

**W SERIES**




| INPUT | OUTPUT |
|---|---|
| + | −3V |
| GRD | GRD |

W512 POSITIVE LEVEL CONVERTER

Positive logic systems, such as those using monolithic integrated circuits, can use the W512 to make available standard DEC levels of −3V and ground to accessory modules in the W and A series.

Input threshold voltage to each converter is normally 1.6 volts for compatibility with DTL and TTL levels. This threshold can be set at 0.8 volts by grounding pin V for RTL level conversion.

**Inputs:** Input current 1 ma or less for input voltages between 0.3 volts and the threshold. 100 μa for inputs above the threshold. Input voltages must not exceed 6.0 volts with pin V open, or 5.3 volts with pin V grounded. Inputs must exceed nominal thresholds by at least 0.4 volts for full switching with minimum noise rejection.

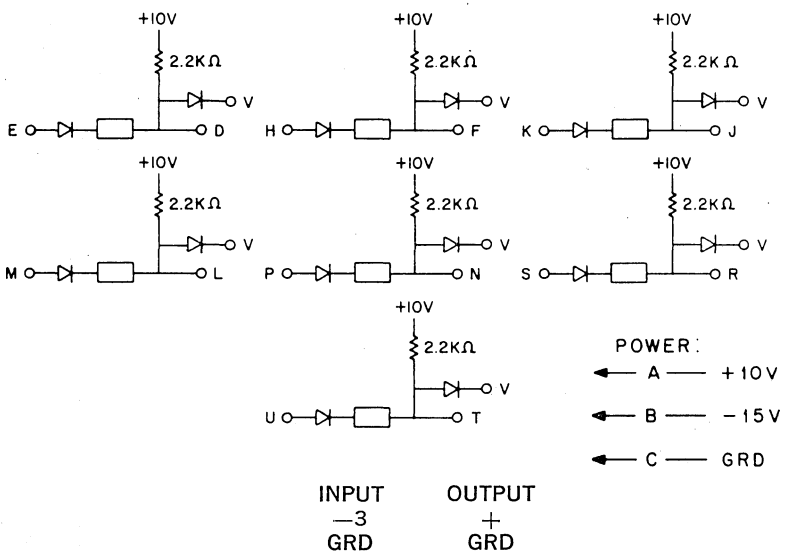
**Outputs:** Each output can supply up to 8 ma at ground. Grounded inputs provide grounded outputs and positive inputs provide negative outputs. Output rise and fall TTT are less than respectively 70 and 200 nsec.

**Power:** 10v (A)/104 ma: 15 v (B)/30 ma.

W512 — $25

# POSITIVE LEVEL AMPLIFIER
## W603

**W SERIES**




W603 POSITIVE LEVEL AMPLIFIER

Positive logic systems such as those using RTL, DTL, or TTL monolithic integrated circuits can be driven from FLIP CHIP systems through the W603. Clamped load resistors at the output of each circuit permit output levels to be adjusted to the type of circuit being driven. This clamp voltage is common to all seven converters on the module.

**Inputs:** 1 ma at ground.

**Outputs:** Each output can supply up to 5 ma at ground. Drive capability at the positive output voltage is provided by internal 2200-ohm resistors returned to +10 volts. The upper positive level will be no more than 0.8 volts above the clamp voltage.

Grounded inputs provide grounded outputs; negative inputs produce positive outputs. Output rise and fall TTT are less than respectively 100 and 150 nsec.

**Power:** +10(A)/35 ma. — 15(B)/7 ma.

When the W603 is used to drive M or K series modules, the module pins V and A may be tied to the +5 volt logic power supply. The following drive capability will result:

Each output will supply one M series unit load, or two K series unit loads.

W603 — $23

This subassembly process depicts the soldering of bussing strips. A high current passes through the bus strip to evenly distribute all solder.

# K SERIES

# K SERIES

## INTRODUCTION

K Series modules were designed to be used in control applications. Their unique characteristics of slow speed (100 KHz maximum) and high noise immunity make them ideal for many industrial applications. Some K Series modules are compatible with the M Series line previously described. In the following pages a brief summary will be made of each K Series module. More elaborate descriptions will be made of those modules which are M Series compatible or which are new to the K Series module line.

Further information on all K Series modules may be obtained by filling out a form provided at the rear of this book; ask for a free copy of Digital's "Control Handbook".

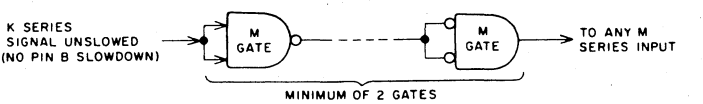
## COMBINING K WITH M-SERIES MODULES

There are several types of applications in which a combination of M and K Series modules is better than either one alone, such as interfacing a K Series system to a computer or interfacing an M Series system to electro-mechanical devices. Here are the things to consider and recommended designs for both pulses and levels in each direction.

## TIMING

Timing considerations are important, but unfortunately are not reducible to simple rules: as in any other logic design task, interfacing K with M Series modules requires adherence to all timing constraints of the output device, the input device, and the logic loops (if any) as a whole. As a minimum, M Series signal driving K Series circuits must last long enough (at least 4 microseconds even if no propagation within the K Series is required) so that the K Series will not reject it as if it were noise; and as a minimum, K Series signals driving M Series circuits must be received by M Series inputs that will not be confused by ultra-slow risetimes.

### K TO M SERIES LEVELS



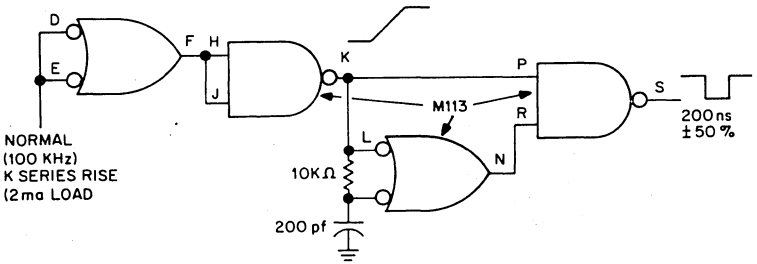

K TO M-SERIES LEVEL CONVERTER

Note: Total lead length connected to input of first M Series gate should be less than 6 inches, to minimize any tendency toward oscillation while active region is being traversed. Do not use slowed K Series levels. If noise still gets through, a .001 capacitor from M Series input pin to ground can be added.

### M TO K SERIES LEVELS

1. Diode gate inputs (K113, K123, etc.) and drivers with flexprint cables (K604, K644, K671) may be paralleled freely with M Series inputs.
2. M Series outputs should not be paralleled (wired AND) with K Series outputs.
3. K303 inputs, K220, K230 readin gate inputs, and K135 and K161 inhibit inputs require the full 5 volt K Series swing, and normally should not be paralleled with M Series inputs. Also in this category are clear inputs to K202, K210, K220, and K230. M Series gate outputs will rise all the way to +5V if no M Series inputs are paralleled with these points, except the K161 inhibit input.
4. Other K Series inputs generally may be driven directly, but in some cases heavy capacitive loading will slow the transitions.

## K TO M SERIES PULSES




Note: Same input restrictions as K to M Series level converter. M113 may be replaced by M602 circuit if desired.

## M TO K SERIES PULSES

Use a type M302 delay multivibrator set for at least 5 μsec (capacitor pins H1-L2 or S1-S2). Observe same restrictions on K Series inputs to be driven as listed above under "M to K Series levels."

**Loading**

Driving M from K Series modules, each risetime-insensitive input should be regarded as a 2ma K Series load, and K Series inputs may be freely mixed with M Series inputs up to the total K Series fanout of 15 milliamperes. M Series inputs could be regarded as 1.6 ma each if more complicated rules and qualifications concerning use with K303 timers and reduction in low-output noise rejection were established, but the 2 ma equivalence is simpler and safer.

Driving K from M Series, each milliampere of K Series load should be regarded as one M Series unit load.

For computer interfacing and other M-Series applications where K Series is used as a buffer to keep noise in the external environment from reaching high-speed logic, beware of long wires between the M and K Series portions. For full noise protection, all signal leads penetrating the noisy environment normally must have K-series modules at both ends. EIA converters (K596, K696) or lamp drivers may offer a helpful increase in signal amplitude or decrease in allowable line impedance for long data links. In any case, use all the slowdown connections or slant capacitors that the required data rates permit.

# MODULE SUMMARY

## GATE EXPANDERS
**K003, K012, K026, K028**

**K SERIES**

K003 — AND Expander: three triple input expanders which may be connected to the AND expansion node of any K Series module.

AND/OR Expander's: three dual input AND gates which may be connected to the OR expansion node of any K Series module.

K012 — OR Expander: three four input OR expanders which may be connected to the OR expansion node of any K Series module.

K026 — AND/OR Expander: three sets of dual input AND gates which are OR'ed into an OR expander gate. The resulting OR'ed output may then be connected to the OR expansion node of any K Series module.

K028 — AND/OR Expander: eight dual input AND gates which are OR'ed into an OR expander gate. The resulting OR'ed output may then be connected to the OR expansion node of any K Series module.

K003 — $5
K012 — $8
K026 — $8
K028 — $8

## LOGIC GATES
**K113, K123, K124**

**K SERIES**

K113 — Inverting Gate: three dual input gates which perform the NAND function. Both AND and OR expansion connections are available.

K123 — Noninverting Gate: three dual input gates which perform the AND function. AND and OR expansion nodes are provided.

K124 — AND/OR Gate: two circuits where two dual input AND gates are OR'ed together. This module provides a convenient method of implementing exclusive OR's, control flip-flops, and two term boolean "OR" equations. It is not expandable.

K113 — $11
K123 — $12
K124 — $14

## INVERTERS
**K134, K135**

**K SERIES**

K134 — Inverting Gate: four inverting gates with a common enable input. These gates may only be AND expanded.

K135 — Inverting Gate: four inverting gates with a common enable input. These gates may only be OR expanded.

K134 — $13
K135 — $13

K161 — Binary to Octal Decoder: Takes a three bit binary number and produces one out of eight lines high.

K161 — $25

K174 — Digital Comparator: This module makes a numerical comparison between two binary numbers and tells which of the two quantities is larger.

K174 — $24

K184 — Rate Multiplier: Module emits a pulse train at an average rate equal to the product of counter and binary fraction inputs.

K184 — $25

## FLIP-FLOPS
**K201, K202, K206**

**K SERIES**

K201 — Flip-Flop: dual set-reset flip-flops for low speed (1 KHz maximum) operation in highly noisy surroundings.

K202 — Flip-Flop: two D type flip-flops whose outputs go to the state of their data inputs when their clock inputs fall from high to low.

K206 — Flip-Flop Register: four set-reset flip-flops with a common read-in enable and direct clear input.

K201 — $39
K202 — $27
K206 — $20

## COUNTERS
**K210, K211, K220, K230, K271, K273, K281**

**K SERIES**

K210 — Counter: a four bit binary or BCD up counter. With expansion gates, it can be connected to count anywhere from 2 to 16.

K211 — Programable Divider: a binary counter which can be wired to produce a high to low output transition after any number of input cycles from 2 to 16.

K220 — UP/DOWN Counter: a binary or BCD UP/DOWN Counter which can be parallel loaded.

K230 — Shift Register: a four bit shift register which can be parallel loaded.

K271 — Set-Reset Retentive Memory: a magnetically latched mercury wetted contact relay flip-flop which can follow important data in a system and retain that data should a power failure occur.

K273 — Retentive Memory: three magnetically latched mercury wetted contact relays which can follow 3 bits of information, and retain that data should a power failure occur.

K281 — Fixed Memory: diode matrix which can code eight four-bit words.

| |
|---|
| K210 — $27 |
| K211 — $20 |
| K220 — $55 |
| K230 — $40 |
| K271 — $40 |
| K273 — $85 |
| K281 — $10 |

## TIMERS
**K301, K303, K323, K333, K371, K373, K374, K375, K376, K378**

**K SERIES**

K301 — Basic Timer: timer circuit which can provide delays ranging from 10 microseconds to 30 seconds. It may be used as an OFF delay, or ONE shot.

K303 — Timer: three delay circuits which provide delays from 10 microseconds to 30 seconds. Delay circuits may be connected to form clocks, with frequency ranges between 2Hz and 6KHz.

K323 — One Shot: three one shot circuits which convert an input transition (high to low) to an output pulse from 10 microseconds to 30 seconds.

K333 — Pulsers: three pulse circuits which produce pulse widths above 10 microseconds. Pulse widths can be varied by adding capacitance to connections provided.

K371 — Timer Controls:
K373
K374
K375
K376
K378

Full complement of timing component boards which bolt directly on timing modules. These timing component boards contain calibrated controls for setting the time required.

| |
|---|
| K301 — $15 |
| K303 — $27 |
| K323 — $35 |
| K333 — $23 |
| K371 — $11 |
| K373 — $11 |
| K374 — $15 |
| K375 — $11 |
| K376 — $15 |
| K378 — $15 |

## MANUAL CONTROLS
### K410, K420, K422, K424, K432

## K SERIES

K410 — Indicator Lights: five indicator lights which can be used to monitor logic level outputs.

K420 — Switches: three manual switches with built in switch filters.

K422 — Thumbwheel Encoders: dual 10 position thumbwheels with circuitry to produce BCD outputs.

K424 — Thumbwheel Decoders: dual 10 position thumbwheels with circuitry to detect any BCD digit.

K432 — Timer Controls: various timing components to be used with K3XX Series modules.

| |
|---|
| K410 — $18 |
| K420 — $33 |
| K422 — $27 |
| K424 — $27 |
| K432 — $33 |

## INPUT CONVERTERS
**K501, K508, K522, K524, K531, K578, K580, K581, K596**

**K SERIES**

K501 — Schmitt Triggers: four circuits which may be connected to noisy signal sources to prevent false triggering. Built in hysteresis and slowed outputs insure reliable operation.

K508 — AC Input Converter: operating through a K716 interface block, this module converts 120 VAC input voltages to logic levels.

K522 — Sensor Converters: two comparator circuits which convert resistance changes and small voltage variations to logic levels.

K524 — Sensor Converters: four comparator circuits which convert resistance changes and small voltage variations to logic levels.

K531 — Quadrature Decoder: quadrature decoder that provides the proper direction and count controls for a K220 UP/DOWN counter register.

K578 — 120 VAC Input Converter: eight circuits which convert 120 VAC inputs to logic levels. The inputs to the converter are through transformers which provide sufficient reactive load to keep contacts clean.

K580, K581 — Dry Contact Filters: these filters are used with wiping type switches and provide a voltage divider to convert high DC voltages to logic levels.

K596 — EIA Input Converter: transforms any bipolar input signal with amplitudes between ±3 volts and ±25 volts into standard K Series or M Series logic signals.

| |
|---|
| K501 — $25 |
| K508 — $44 |
| K522 — $25 |
| K524 — $98 |
| K531 — $70 |
| K578 — $80 |
| K580 — $28 |
| K581 — $20 |
| K596 — $20 |

## OUTPUT CONVERTERS
**K604, K614, K615, K644, K656, K658, K671, K681, K683, K696**

**K SERIES**

K604 — Isolated AC Switch: four switching circuits, which allow logic levels to control AC devices, such as, solenoids, AC valves, small motors, and motor starters. Each switch can handle 250 volt amperes.

K614 — Isolated AC Switch: four switching circuits which allow logic levels to control AC devices, such as, solenoids, AC valves, small motors, and motor starters. Each switch can handle 500 volt amperes.

K615 — Isolated AC Switch: four switching circuits which allow logic levels to control AC devices, such as, solenoids, AC valves, small motors, and motor starters. Each switch is rated at 500 VA and provides a fail-safe against accidental removal of modules or cut wires that connect directly to the AC switch input.

K644 — DC Driver: four switching circuits used to switch stepping motors, DC solenoids and similar devices rated up to 2.5 amperes at 48 volts.

K656 — DC Driver: four switching circuits used to switch stepping motors, DC solenoids and similar devices rated up to 1 ampere at 250 volts.

K658 — DC Driver: four switching circuits used to switch stepping motors, DC solenoids, and similar devices rated up to 4 amperes at 125 volts.

K671 — Decimal Decoder and NIXI Display: contains a side viewing Burroughs type nixi glow tube, and a decimal decoder. One K771 power supply is needed for each 6 nixi displays.

K681 and K683 — Lamp Drivers: eight circuit modules which can drive external resistive and inductive loads. They are used primarily to drive incandescent lamps.

K696 — EIA Output Converter: six bipolar non-inverting driver circuits which convert standard logic levels to either American EIA or European CCITT signals for data transmission.

| | |
|---|---|
| K604 | $110 |
| K614 | $ 88 |
| K615 | $ 92 |
| K644 | $ 66 |
| K656 | $ 80 |
| K658 | $128 |
| K671 | $ 55 |
| K681 | $ 15 |
| K683 | $ 30 |
| K696 | $ 44 |

## INTERFACE HARDWARE
### K716, K724

K SERIES

K716 — Interface Block: interconnection interface for those K-Series modules that communicate with external equipment. External field wiring terminates at a 24-terminal screw connection block that accepts plain stripped wire up to 14 gauge.

K724 — Interface Shell: shell which provides the connectors and mechanical support for self-contained interface modules, K578, K604, K614, K615, K656 and K658.

| | |
|---|---|
| K716 | $75 |
| K724 | $55 |

# POWER
## K730, K731, K732, K741, K743

**K SERIES**

K730 — General Purpose Module: the K730 can be used with any +5 VDC power supply to generate the turn on and power OK signals. It also rectifies 12.6 VDC to approximately 16 VDC and 10 VDC.

K731 — Source Module: supplies +5 VDC power to pin A of all K Series modules and provides several specialized once-per-system control functions.

K732 — Slave Regulator: this module is normally tied to pins of a K731 source. For each unit of current emitted by the K731 the K732 emits two. Up to three K732 slaves can be controlled by a single K731 for a total system current of 7 amperes.

K741 and K743 — Power Transformers: these hash-filtered, 50/60 Hz transformers supply K731 source and K732 Slave Regulator modules. The K743 also provides an auxiliary 12 VAC winding for use with K902, K508, K681, K683 and K730 modules.

K730 — $19
K731 — $30
K732 — $27
K741 — $30
K743 — $45

K771 — Display Supply: the K771 supplies power and a convenient two screw mounting for up to six K671 display tubes.

K771 — $35

K782 and K784 — Terminals: these modules offer an alternative to the K716 for obtaining field wiring connections in K Series systems. The K782 has straight-through connections for use with K508, K524, or K644 modules. The K784 includes 60 v clamp diodes for protection of K681 or K683 modules driving inductive loads.

K782 — $12
K784 — $17

K791 — Test Probe: pocket test probe contains two pulse-stretching lamp drivers for visual indication of both transient and steady-state conditions.

K791 — $40

K940 and K941 — Mounting Hardware: K940 is a mounting support that attaches to the enclosure. K941 is a removable bracket that mounts up to four H800 connector blocks.

K940 — $4
K941 — $6

K943-R- and K943-S-19″ Mounting Panel: these 19″ panels have sixty-four 18 pin connector sockets with either wire-wrap (R) or solder fork (S) contact pins.

K943-R- — $96
K943-S- — $96

K950 — Modular Panel Hardware: the K950 provides a convenient way to build control panels containing lights, toggle and push button switches, timer controls and thumbwheel switches. The lower connector half of the control modules, K410, K420, K422, and K432 are plugged into the upper connectors across a K943 mounting panel and the manual controls protrude through the K950 panel frame.

K950 — $39

K980 — End Plates: pair of plates for supporting 1907 cover to hold modules in K943 panel under shock and vibration.

K980 — $6

K982 — Mounting Panel: the K982 is a predrilled 19″ mounting panel on which can be mounted up to three separate power transformers (K741 or K743).

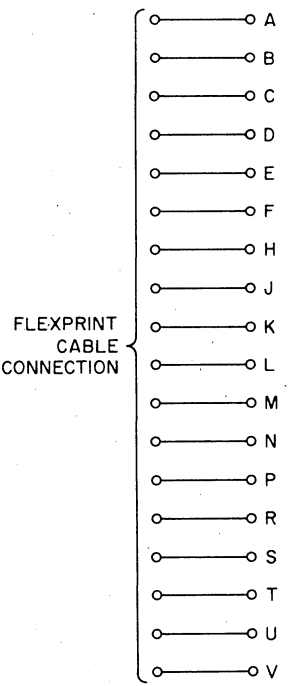
K982 — $10

K990 — Timer Component Board: the K990 is a predrilled etched module for mounting up to six RC networks for K301, K303 or K323 timer controls.

K990 — $4

# NEW K SERIES PRODUCTS

| CABLE CONNECTOR<br>K080 | K<br>SERIES |
|---|---|

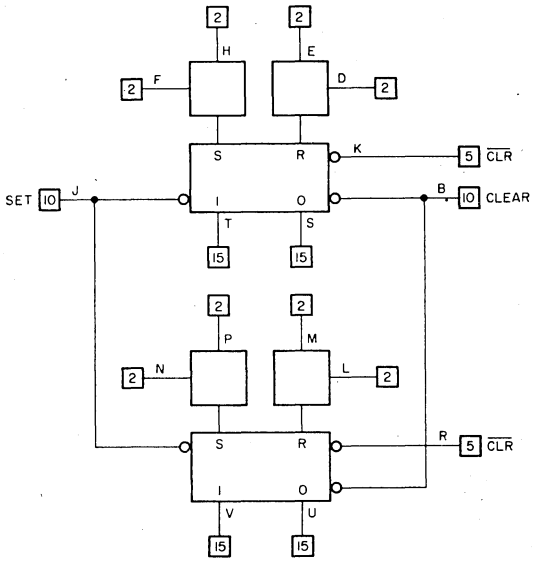



The K080 cable connector consists of a single height, single thickness board on which can be mounted a 19 conductor flexprint cable. Each module comes with a cable clamp for customer convenience.

K080 — $3

# FLIP-FLOP
## K201

**K SERIES**




This superslow memory simplifies sequencing of machine motions, and finds other applications where the ultimate in noise isolation is needed and speed is no problem. Its 1 KHz maximum repetition rate makes this flip-flop noticeably more resistant to extremely noisy surroundings than faster types like K202, K210, etc. So noise immune, in fact, that several yards of wire may be connected to K201 outputs even in severely noisy areas without errors.

The K201 flip-flop input gating is designed to respond to the time sequence of two inputs rather than to their simple AND function. Level inputs E, H, M, and P must be high at least 400 $\mu$s before the pulse inputs D, F, L, and N make a high to low transition. The flip-flop will compliment if the S and R inputs are pulsed at the same time. The input minimum noise rejecting time thresholds are 100 $\mu$s. Successive input transitions must not be closer than 400 $\mu$s.

Grounding pin J causes pins T and V to go high and pins S and U to go low, regardless of the state of any other input pins.

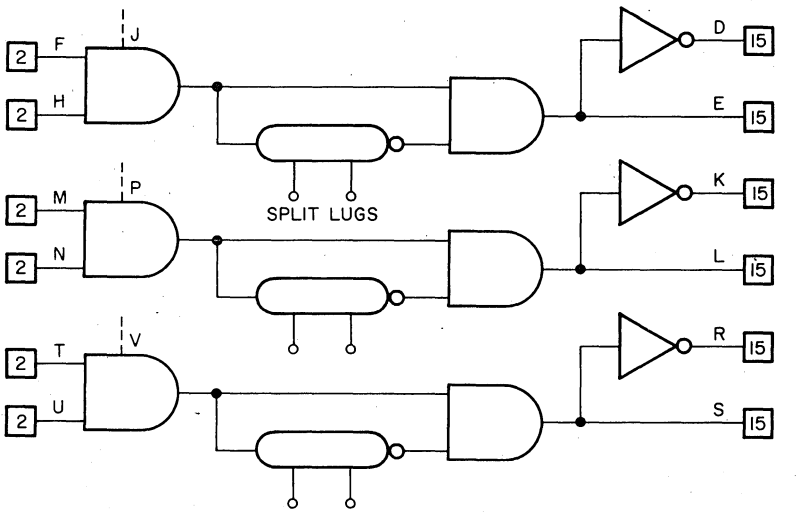
Each flip-flop circuit on this module has a separate clear input (Pins K and R). If either of these inputs is grounded the ZERO output of that specific flip-flop will go high and the ONE output will go low.

There is also a common clear, Pin B, which when grounded, forces Pins S and U high and Pins T and V low.

K201 — $39

# PULSERS
## K333

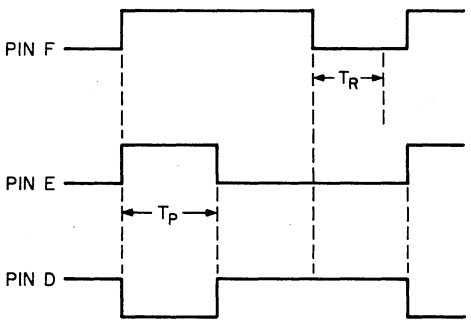
**K SERIES**




The K333 Pulser circuits are designed to produce pulses from low to high level transitions. The length of a pulse is determined by the capacitance connected to split lugs conveniently mounted on the module.

Without a capacitor connected to the split lugs, the K333 Pulser circuits give a 10 to 15 microsecond pulse. For each .001 $\mu$f capacitor connected to the split lugs, the pulse width increases by approximately 10 microseconds. A minimum recovery time ($T_R$) of 2000C seconds, where C is the value of the capacitance used, should be allowed to ensure 95% repeat accuracy in the output pulse width. All inputs to these circuits must be longer in duration than the output pulse widths desired. Complimenting outputs are also provided on each circuit.

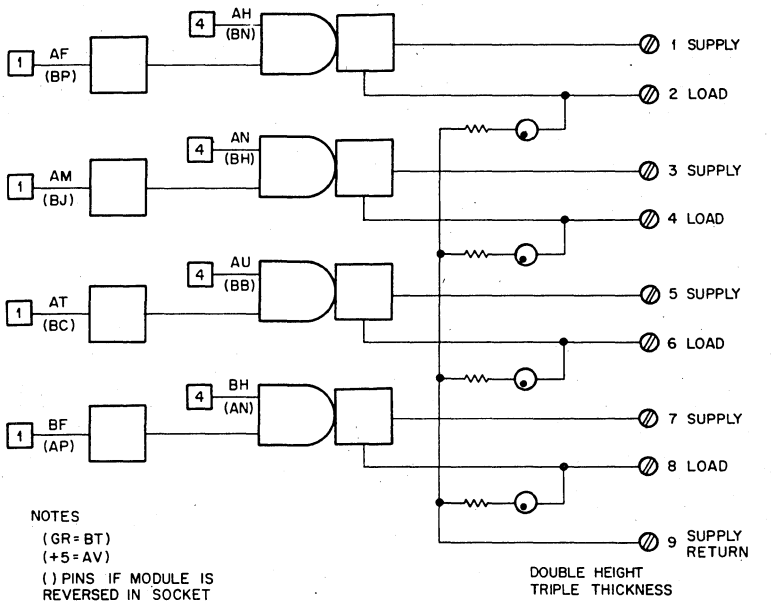
Typical outputs for a given input are shown below:




Hysteresis at the inputs makes it possible to use the outputs of the K578, K580 and K581 modules as inputs. The AND expansion node may be used with a K003 to generate pulses from a counter. Even though each pulser may have a different timing capacitor, it is recommended that all circuits be given the same width on all modules so that modules may be interchanged without creating logic timing problems.

# ISOLATED AC SWITCH
## K615

**K SERIES**

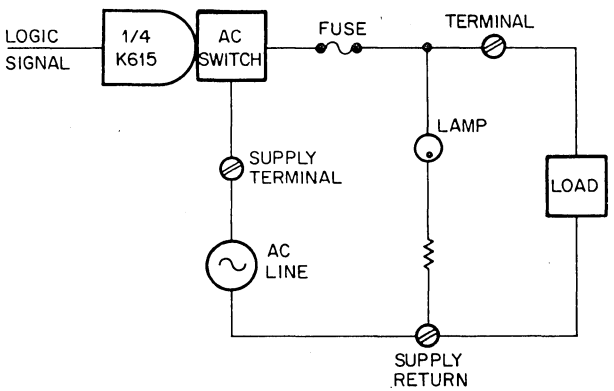



### K615 AC SWITCH

The K615 uses the same switching circuits as the K614. The difference between the K614 and K615 is in the input circuits. One input on each circuit of the K615 (AF, AM, AT, and BF) normally assumes the logic "0" level when it is open circuited. This is contradictory to all other K Series inputs which normally assume a high level when no input is connected.

Because the switch turns on when both inputs are high, this feature provides an additional fail-safe against the accidental removal of modules or cut wires that connect directly to the AC switch input. If the protected input is unused, it must be wired to pin A.

The K615 has built-in clamp-type terminals for wires to size 14, interchangeable indicators, and fused outputs rated at 500 VA per circuit. Fuses are 5 AMP Littlefuse type 275005.

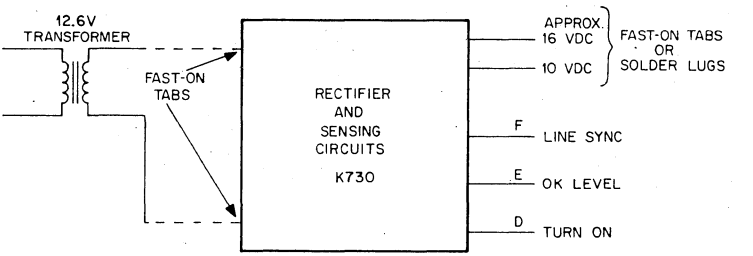



K615 CIRCUIT IN USE

K615 — $92

# GENERAL PURPOSE MODULE
## K730

**K SERIES**




The K730 is a general purpose module that can be used with any +5 volt power supply to generate the turn on and power OK signals that are normally provided by the K731.

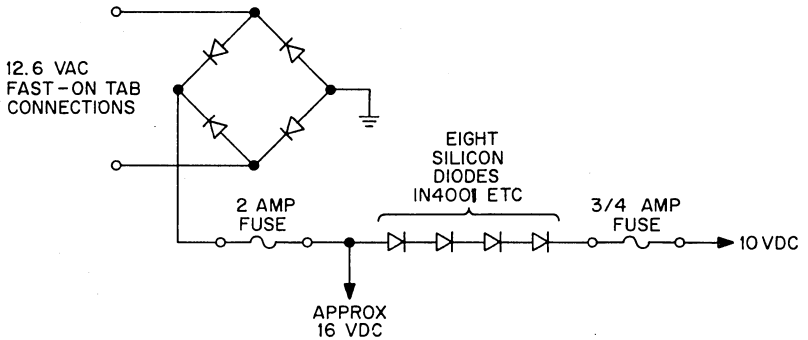
If an external 12.6 volt transformer is connected to the fast-on tabs at the handle end of the module, a 2 amp diode bridge power supply and a line sync will also be available.

The line sync output on pin F allows a K113 or K123 gate to switch in synchronism with ac supply zero-crossings. This permits the line frequency to drive a realtime clock, or serve as the standard in a phase-locked loop with K303 timers, where higher frequencies must be synchronized with the line. Line sync fanout is limited to 1 ma (for high fanout, use K113 or K123 for distribution).

The bridge power supply has two separate fused outputs. The direct output is fused for 2 amps and the diode string output is fused for ¾ amps. The diode string output may be used with the K580 switch filter as a source of +10 volts for contact sensing. Space is provided on the board for an electrolytic capacitor to be added if a filtered supply is desired. All supply outputs are brought out through fast-on tabs at the handle end of the module. The auxiliary winding on the K743 transformer may be used, however, any 12.6 VAC transformer may be used as long as it does not have a grounded center tap.

The turn-on output on pin D goes to ground during the power-up transient and remains at ground until at least 5 ms after the supply voltage has reached its quiescent value. It may be used to initialize flip-flops to a known voltage.

The OK level output (pin E) goes to ground when the +5 VDC supply voltage at pin A reaches 4.5 volts, and returns positive when less than 4.5 volts is available. It is normally used as an enabling input to the K273 Retentive Memory module.

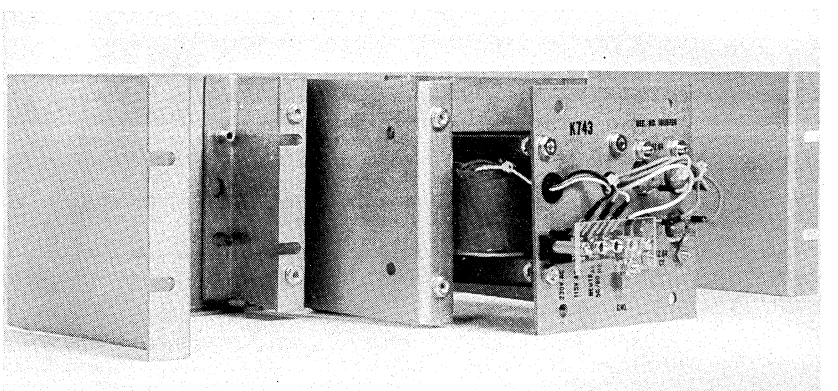



GETTING APPROXIMATELY +16 VDC AND +10 VDC
FROM K730

K730 — $19

# MOUNTING PANEL
## K982

**K SERIES**




The K982 is a predrilled 19″ mounting panel on which can be mounted up to three separate power transformers (K741 or K743).

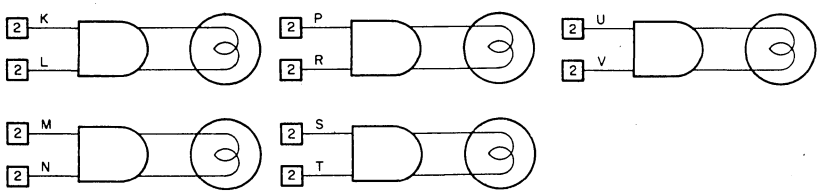
Transformers can be mounted using either the K980 end brackets for exposed transformer connections or H002 setback brackets for unexposed transformer connections.

K982 — $10

# M SERIES
# COMPATIBLE MODULES

## INDICATOR LIGHTS
K410

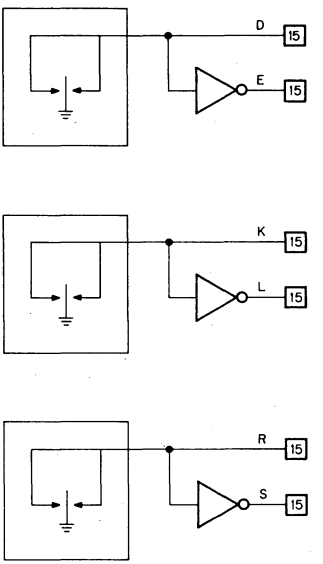
K SERIES




The K410 indicator lamp module provides a convenient way to build binary, decimal, octal, or bi-quinary displays. Lamps and lamp drivers receive their supply voltage through fast-on tab connectors. Any 12.6 V c. t. transformer may be used as a voltage supply provided the center tap is grounded.

The K410 may be used in a K943 mounting panel with or without the K950 panel hardware. Inputs are located on the B connector half of the module. Two modules plugged side by side on ½ inch centers provide 10 lamps for decimal, octal, or bi-quinary displays. More modules may be plugged in to provide five horizontal binary registers. Lamps turn on when both inputs are high or left unconnected.

K410 — $18



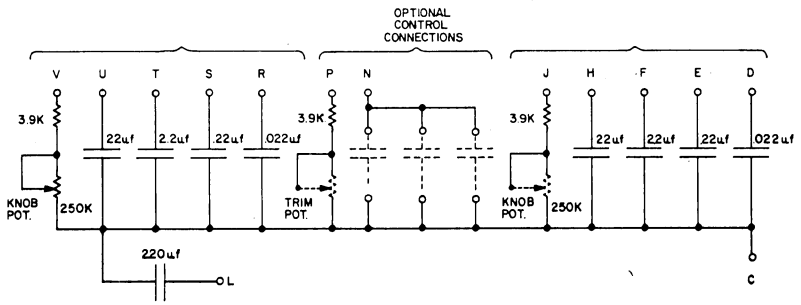

The K420 uses three 3-position Toggle switches. Only when the Toggle is in the center position will pins D, K, and R be high. The switch acts like a SPST Toggle in one direction and a spring returned push button in the other direction. Built in switch filters and Schmitt Triggers remove all switch contact bounce. Both inverted and uninverted outputs for each switch can drive 15 unit loads. Outputs are unslowed and may be used to drive M Series inputs directly.

The K420 may be used in a K943 mounting panel with or without the K950 modular panel hardware. All connections are made on the B connector half of the module.

K420 — $33

# TIMER CONTROL
## K432

**K SERIES**




The K432 Timer Control module used with a K301, K303, or K323 allows timer delays to be adjusted from a front panel by rotating a knob-pot. Timing ranges are selected by connecting the desired capacitor as shown in the table below either with wire wrap or 913 grip clip patch cords.

The board is predrilled and etched to provide space for a screw driver adjustable trimpot and capacitor to be mounted to obtain a third timer control. Each capacitor on the board may only be connected to one RC timer circuit at a time, however, any capacitor or resistor may be connected to form an RC.

The capacitor on pin L may be used with either the upper or lower knob-pot to obtain a range of 1 to 30 seconds.

Pins J, P, or V are connected to the RC time pins on the timer modules.

| Connect to Pin J or V | RC Time Range Min. | Max. |
|---|---|---|
| None | 10 $\mu$s | 300 $\mu$s |
| D or R | 100 $\mu$s | 3 ms |
| E or S | 1 ms | 30 ms |
| F or T | 10 ms | 300 ms |
| H or U | 100 ms | 3 sec |
| L | 1 sec | 30 sec |

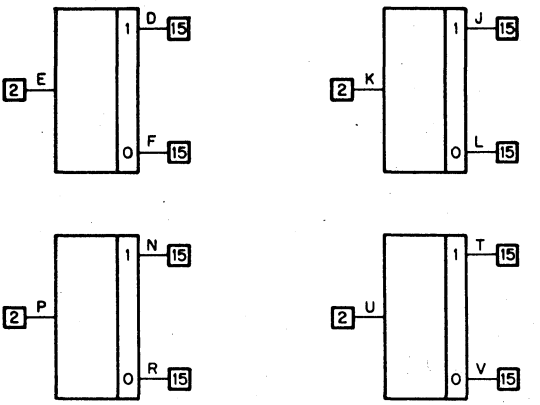
Pin connections for selecting time ranges.

The K432 is designed to be used with or without the K950 modular hardware panel. All connections are on the B connector half of the module.

K432 — $33

# SCHMITT TRIGGERS
## K501

**K SERIES**



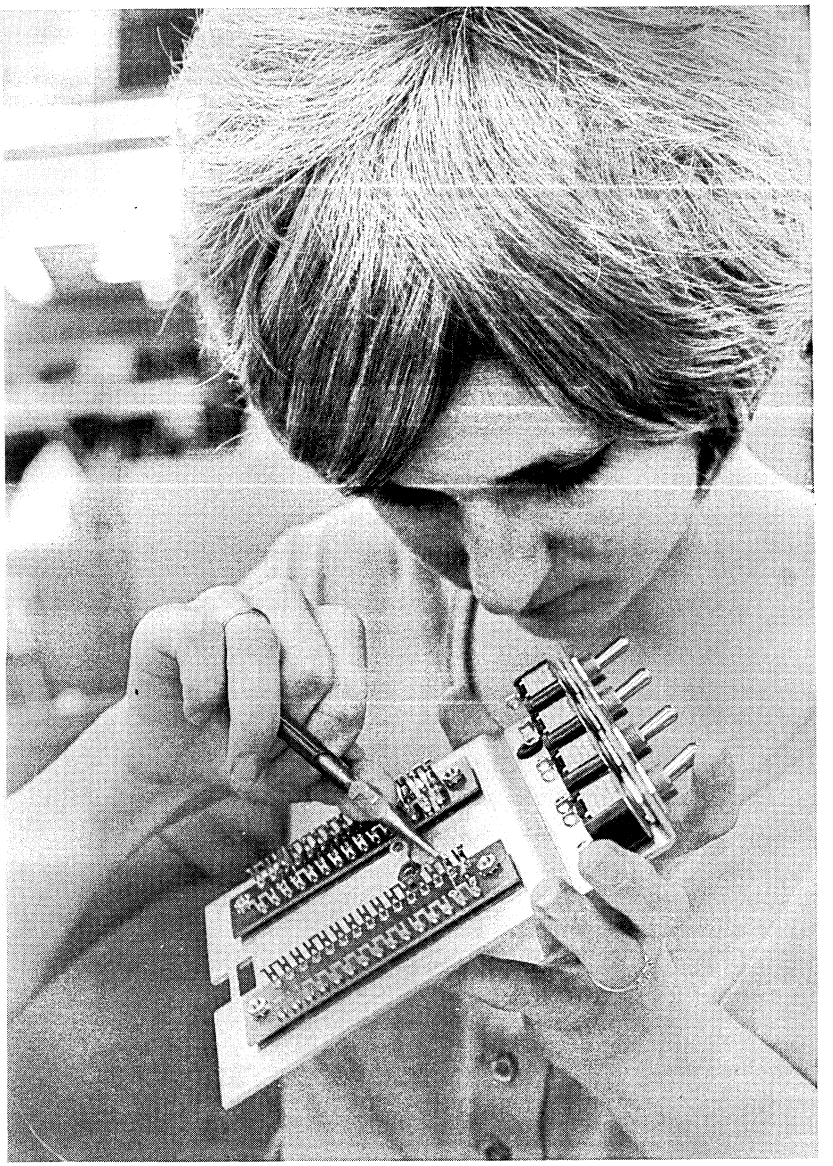

The K501 can be used with the K580, K581, or K578 to provide simultaneous true and complement signals with full K series drive. Built in hysteresis and slowed outputs insure reliable operation in noisy signal environments.

Schmitt Triggers can also be used to speed up signals with very slow rise or fall times for input into pulse formers or logic circuits where timing considerations are critical.

The K501 is not designed to be connected directly to unfiltered contacts or other noisy signal sources. The Schmitt Triggers have standard K-Series outputs and their rise time is on the order of 7$\mu$s. Minimum hysteresis between upper and lower Thresholds is 1 volt.

A logic "1" level at pins E, K, P and U forces pins D, J, N, and T high and pins F, L, R, and V low. A logic "0" level at pins E, K, P and U forces pins D, J, N, and T low and pins F, L, R, and V high.

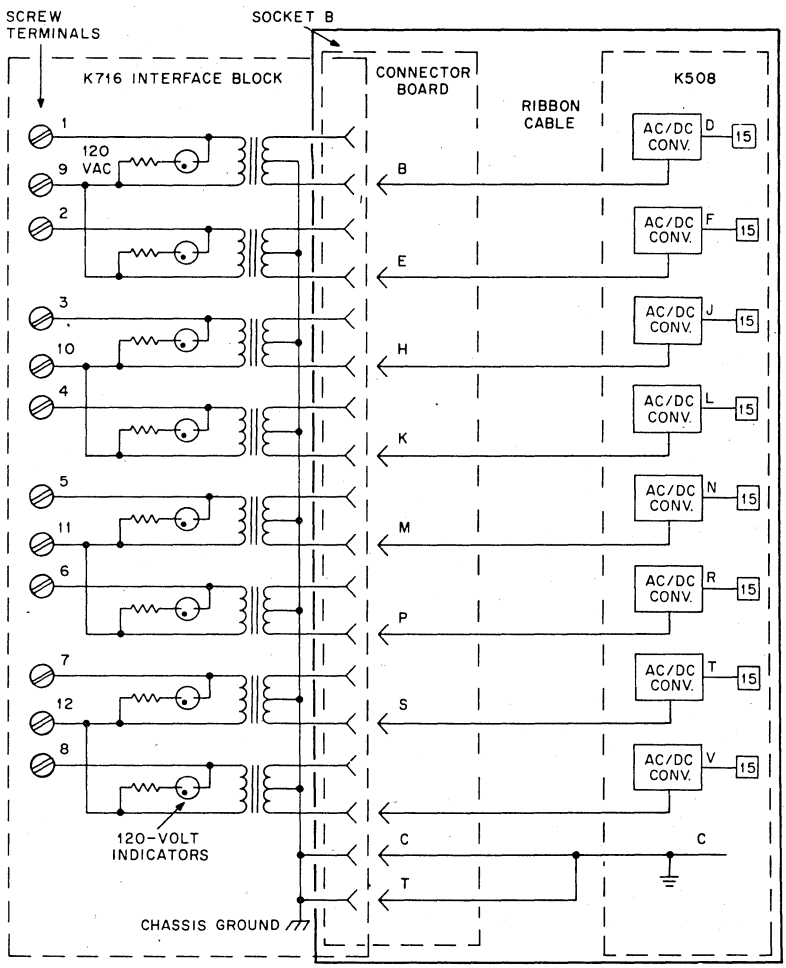
K501 — $25



This subassembly process shows the placing of components and jumpers on a specially prepared terminal strip.

# AC INPUT CONVERTER
## TYPE K508

**K SERIES**



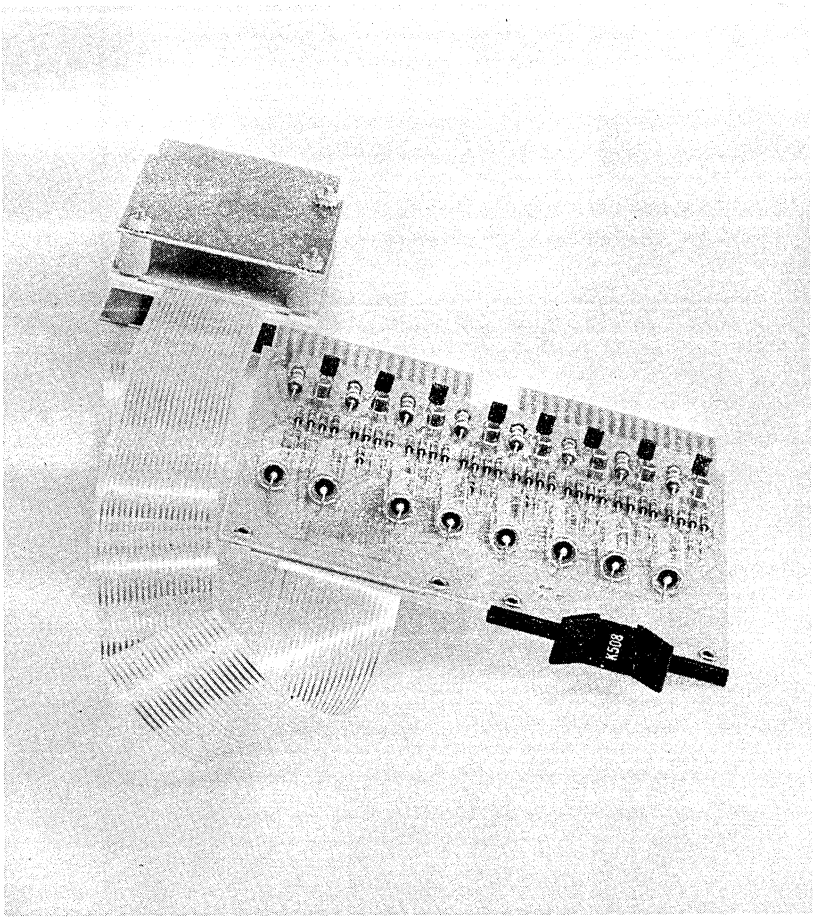

**DOUBLE HEIGHT**

K508 — $44

The K508 AC input converter, operating through the K716 interface block, is designed for use with ordinary silver contacts in limit switches, pressure switches, pushbuttons and the like. Each input terminal presents a reactive load of 1 volt-ampere, which together with an external 120 volt AC pilot circuit voltage inhibits contamination buildup at the contact surface.

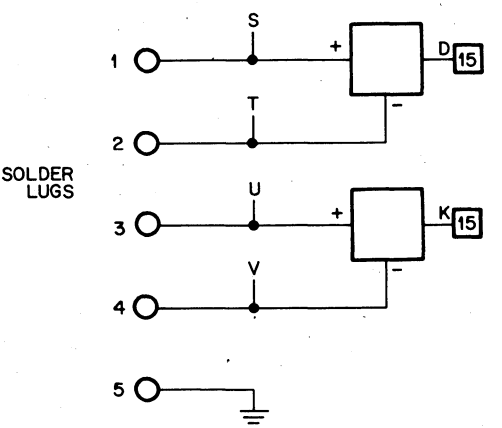
Electrical noise riding on pilot circuit wiring is attenuated in the input transformers and by hash filters at the K508 module. Contact bounce filtering is designed to respond to the first signal, and to leave the logic output in the "1" state in spite of skips lasting up to 100 milliseconds.

K508 output circuits have hysteresis, so that no intermediate output state can result from an ill-defined input condition. No separate Schmitt-triggers are required. Outputs are at ground for no input, at +5 volts when energized. All connections use upper connector.



# SENSOR CONVERTER
## K522

**K SERIES**




K522 SENSOR CONVERTER

The K522 Sensor Converter is basically a voltage comparator that compares an unknown variable input voltage against a fixed internal threshold voltage (+1.8 v). This module can also be converted to a resistance sensing device by mounting a three prong trimpot in the predrilled holes provided in each circuit.

**Voltage Sensing** — This circuit has a built-in reference voltage of +1.8 volts, programmable hysteresis and noise cancelling ability. The K522 does not, however, provide the tolerance to high level noise or accidental application of line voltage which is obtainable from the K524.

If the unknown voltage applied to the K522, is higher than the reference voltage, the comparator output will be a logic 1. If this applied voltage, however, is less than the reference (+1.8 v) the output will be a logic 0.

The minus input to each converter is AC coupled to the internal +1.8 volt reference to provide common mode noise rejection (CMR). In order to be effective, it must be connected to the same ground point to which the Transducer is connected. Twisted pair wiring should be used between the Transducer and Converter to help insure that any noise pick up will be the same on both wires (this is common mode noise).

| CHARACTERISTICS | K522 |
|---|---|
| Number of circuits | 2 |
| Module height and thickness | single |
| Input connections | solder lugs |
| Inputs accessible at module connector | yes |
| DC differential mode possible | no |
| Provision for adding transducer biasing trimpots in predrilled holes on board | yes |
| Noise cancellation range (common mode) | ±1 volt |
| Maximum + input range for correct output | 0 to +5V |
| Tolerance to overvoltage (no damage) | ±3 volts |
| Minimum hysteresis | 10mv |
| Maximum hysteresis | 160mv |
| Minimum transducer resistance (at threshold) | 400Ω |
| Maximum transducer resistance (at threshold) | 20KΩ |
| Noise Cancellation ratio at Line Frequency (CMR) | 10:1 |
| Noise Cancellation ratio at 1 KHz | 20:1 |
| Temperature Coefficient of Threshold (typical) | ±1mv/°C (0.1%) |

**RESISTANCE SENSING** — With a trimpot mounted, the K522 becomes a resistance sensor. The circuit automatically provides a +3.6 volt bias to the trimpot. The resistance of the trimpot can be adjusted to equal the transducer resistance at the desired sensing point. Only when the resistance of the transducer is greater than the resistance of the trimpot will the sensor converter output go high.

In general, the K522 is suited to laboratory and light machinery use where transducers are nearby and there is little danger of high voltage being applied to them accidentally. This is especially important when low resistance transducers are used with board mounted trimpots, since the trimpot provides a path from the transducer leads back to the logic supply. (If high voltage such as 120 VAC) were to get to the logic supply, all modules in the system would be destroyed.

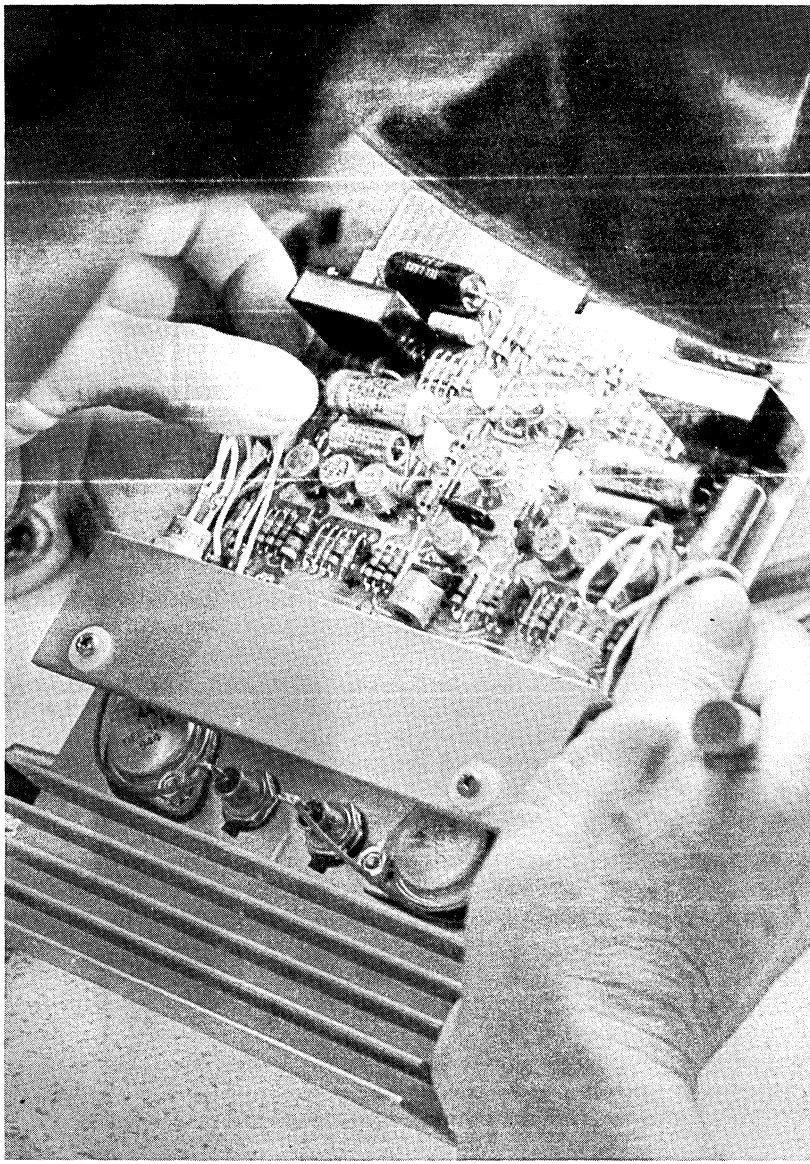
The hysteresis of each K522 circuit can easily be selected in increments of 10 mv from a minimum of 10 mv (no connection) to a maximum of 160 mv by connecting one or more programming pins to the output.

Below is a table of pin connections for programming the hysteresis of each circuit.

| Value when wired to converter output | 10mv | 20mv | 40mv | 80mv |
|---|---|---|---|---|
| Circuit 1 (Pin D) | E | F | H | J |
| Circuit 2 (Pin K) | L | M | N | P |
| Table of Hysteresis Programming Pins | | | | |

Example: To add 30 mv hysteresis to the basic 10 mv hysteresis for a total of 40 mv hysteresis, connect pins E and F or L and M to the circuit outputs.

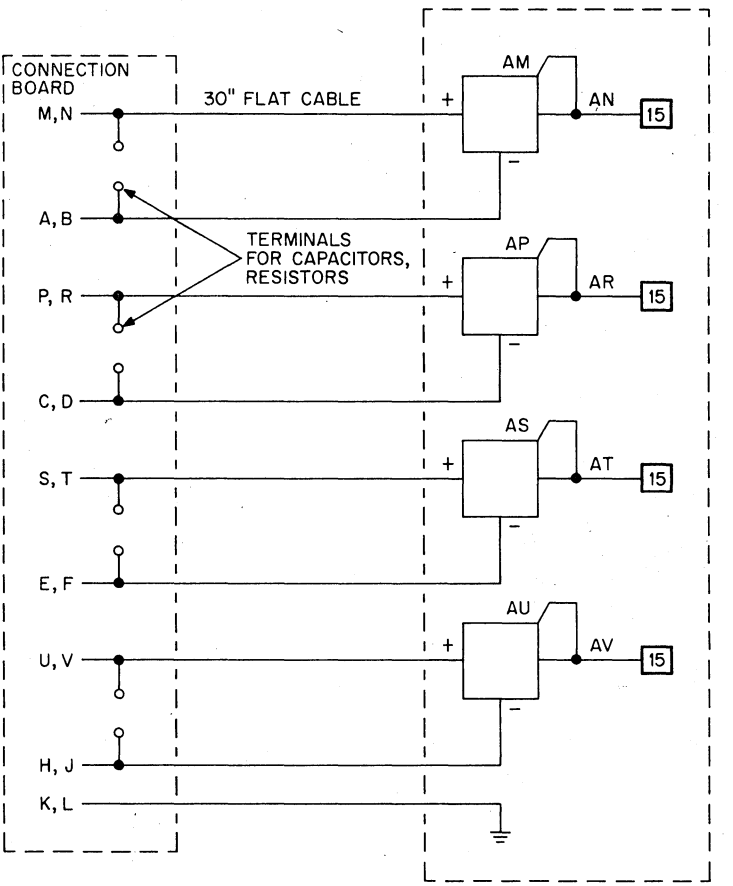
K522 — $25



All DEC modules are exhaustively inspected and tested, both visually and electronically. A typical module undergoes a printed circuit board inspection procedure that consists of over 70 individual steps.

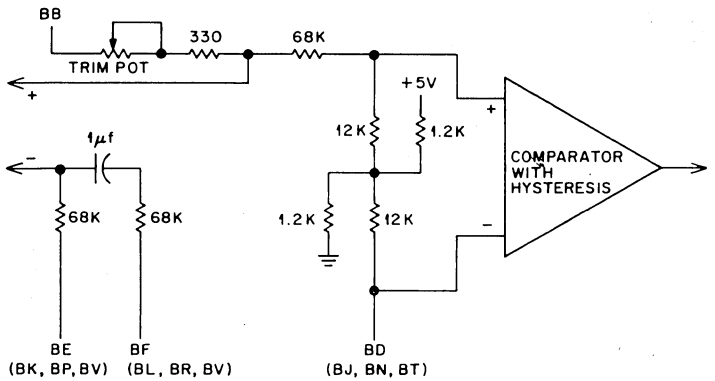
# SENSOR CONVERTER
## K524

**K SERIES**




Basically a noise-rejecting, threshold sensing differential voltage amplifier, the K524 is readily adapted to sensing threshold points in DC analog signals, AC signals, and pulses. It can also be biased to sense resistance thresholds. The differential amplifying technique permits flexible grounding and shielding methods to accommodate floating signal generators and minimize noise.

**VOLTAGE SENSING** — The K524 provides a choice of either AC or DC coupling for voltage sensing.




K524 EQUIVALENT CIRCUIT

The following table shows the auxiliary pin connections on the lower module connector for the various applications of the K524.

| APPLICATIONS | COUPLING | PIN CONNECTIONS |
|---|---|---|
| As low performance analog comparator, for comparing two photocells etc., or wherever reference is supplied externally. | DC | BD to BE, BJ to BK, BN to BP, BT to BV |
| Photocells, thermistors, pulse tachometers, pressure transducers or wherever it is convenient to use the internal 2.5 volt reference. | AC | BD to BF, BJ to BL, BN to BR, BT to BV |

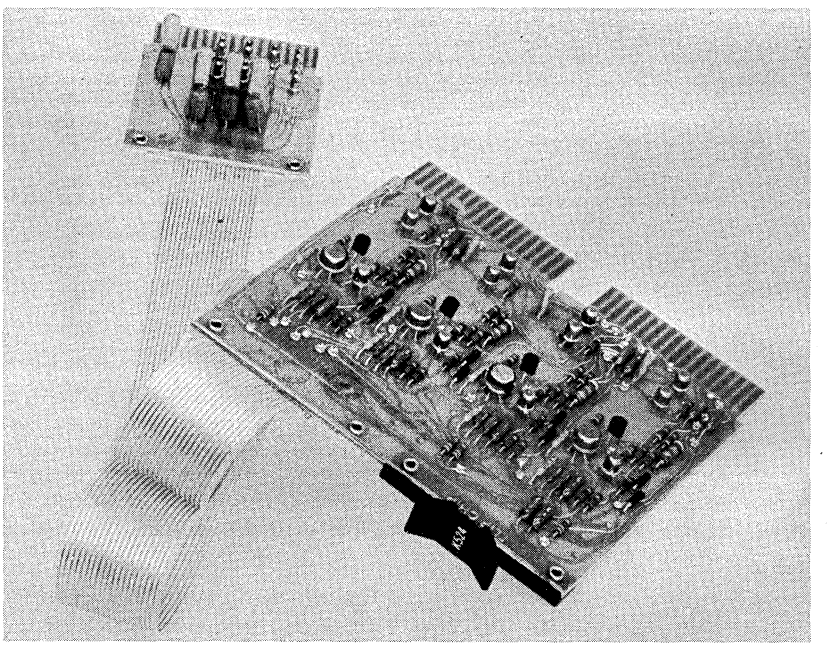
This module has an internal reference voltage of +2.5 volts. If the voltage swings of the unknown voltage applied to the K524 at its (+) input do not go above the internal reference supply voltage of the sensor, an external reference supply will be needed. This reference is applied to the (−) input. DC coupling should also be connected. If the unknown voltage does not go below the internal reference voltage, voltage divider techniques will have to be used.

Output transitions occur when input voltage differentials are within 0.3 volts or less of the reference supply. When the "+" input is more positive, the output is a ONE. When the "+" input is more negative, than the reference, the output is a ZERO.

Signals up to 25 KHz, suitable for counting by K210, K211 or K220 counters, can be obtained with symmetrical input signals having at least 1 volt excursions past the switching point. Maximum output rates can be limited to approximately 5KHz by tying together pins AM and AN, AP and AR, etc.

**RESISTANCE SENSING** — The K524 may be used to sense resistance by mounting a trimpot in the predrilled mounting holes provided. When trimpots are used, pin BB must be connected to an independent +5 VDC bias supply, such as, a separate K731 operated from a separate transformer, to insure against damaging currents through the bias circuits to the logic in case of accidental high voltages at K524 inputs. This precaution is most essential in systems containing K604 or K644 output converters, since inadvertent use of the wrong K716 socket is possible. This problem does not arise with self-generating sensors or where bias is supplied externally to variable-resistance sensors.

When the reistance of the transducer is greater than the resistance of the trimpot the output of the sensor converter will be high. The outputs of the sensor converters will go low when the transducer resistance drops below that of the trimpot.



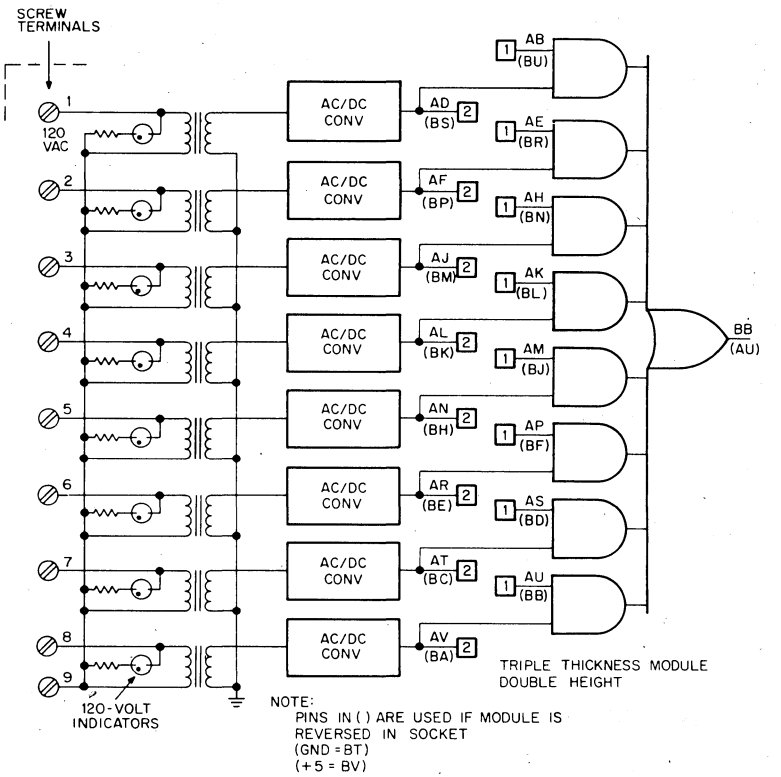
**K524 SENSOR CONVERTER**

| CHARACTERISTICS | K524 |
|---|---|
| Number or circuits | 4 |
| Module size | double |
| Input connections | cable connector |
| Inputs accessible at module connector | no |
| DC differential mode possible | yes |
| Provision for adding transducer biasing trimpots in predrilled holes on board | yes |
| Noise cancellation range (common mode) | ±7.5 volts |
| Maximum + input range for correct output | ±30V |
| Tolerance to overvoltage (no damage) | 140 VAC |
| Minimum hysteresis | 10mv |
| Maximum hysteresis | 10mv |
| Maximum switching rate | 25KHz |
| Minimum transducer resistance (at threshold) | 400Ω |
| Maximum transducer resistance (at threshold) | 100KΩ |
| Noise Cancellation ratio at Line Frequency (CMR) | 10:1 |
| Noise Cancellation ratio at 1 KHz | 20:1 |
| Temperature Coefficient of Threshold (typical) | ±1mv/°C (0.1%) |

K524 — $98

# 120 VAC INPUT CONVERTER
## K578

**K SERIES**




NOTE: PINS IN ( ) ARE USED IF MODULE IS REVERSED IN SOCKET
(GND = BT)
(+5 = BV)

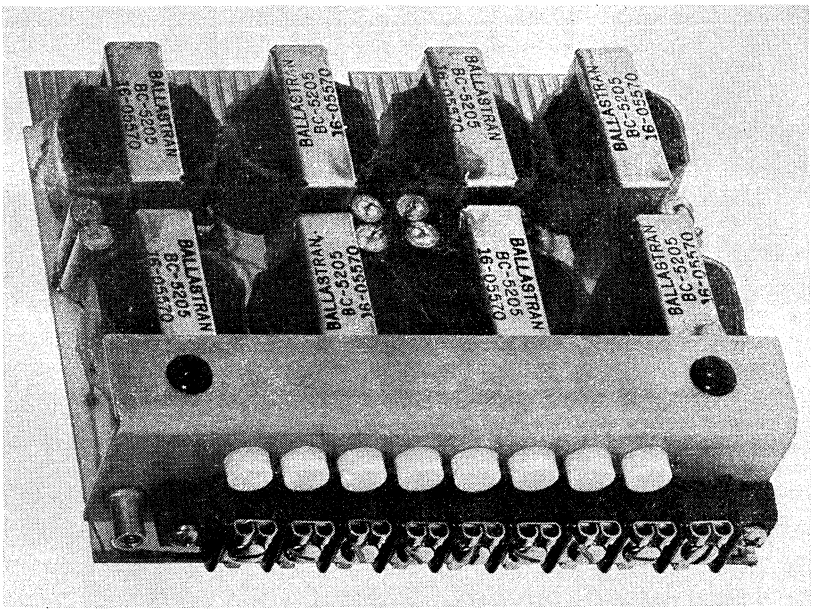
K578 — $80

The K578 input converter, when mounted in a K724 interface shell, provides logic levels from 120 VAC signals from limit switches, relays etc. The 1 VA reactive load provided by the K578 isolation transformers insures sparking at pilot contacts. Together with the ample circuit voltage used, this reactive load assures maximum contact reliability.

Electrical noise riding on pilot circuit wiring is attenuated both by the input transformer and by RC filtering. Bounce filtering is designed to pick up by the end of the first full cycle of contact, and to drop out (return to "zero" output state) by the end of three full cycles after the input is removed. (About 50 milliseconds.) This speed of response is desirable in large sequential scanning-type control systems, even though occasionally a heavy contact may be observed to produce more than one output transition due to very long bounce duration. If necessary, response speed may be cut in half by tying 150 mfd from the offending logic output to ground. However since no Schmitt triggers are included in the K578 (unlike the K508), a K184 or K501 must be used as described in the applications notes if it is important to know exactly how many contact closures have occurred in a given period.

Gating circuits equivalent to four K026 sections are included for contact scanning applications using the K161, or to facilitate forming the logical OR of many inputs. Direct outputs are from circuits similar to the K580, and may not be wired together.

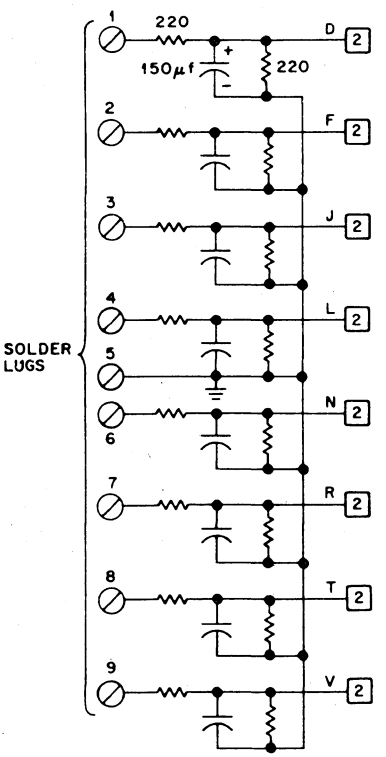
Clamp-type terminals on the K578 take two wires up to size 14. Neon indicators are included. The K578 can also be used in the K943 mounting panel, however some mechanical means of support must be provided to hold the K578 in its socket if vibration is a consideration.



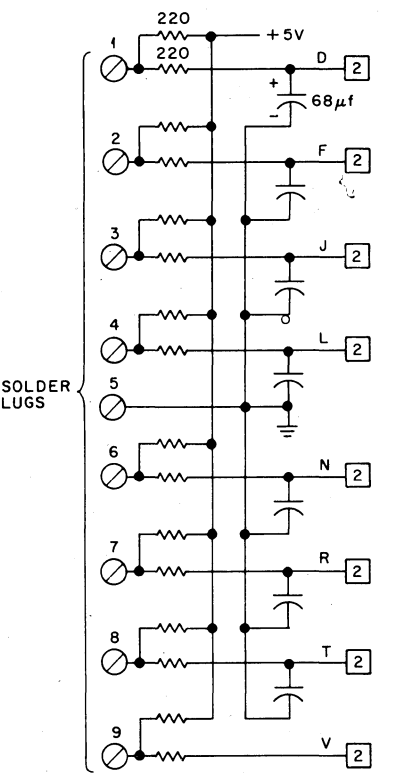

**K578 TERMINAL STRIP CONNECTIONS FROM LEFT TO RIGHT ARE NUMBERS 1 TO 9**

# DRY CONTACT FILTERS
K580, K581

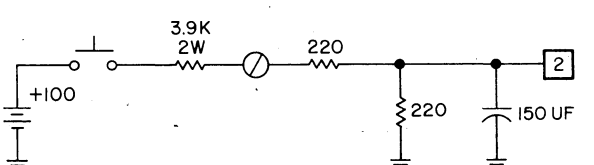
**K SERIES**




**K580**




**K581**

These filters convert signals from dry circuit or wiping contacts to logic levels. Primarily they are used with gold contacts such as the new encapsulated reed limit switches, thumbwheel switches, and the like. Those push-buttons or slide switches that provide good wiping action will also operate reliably with these filters, but silver contacts designed for long life on heavy duty loads are likely to give trouble. For them, use interfaces designed for such application like K508-K716 or K578, or at least switch a high voltage. (see K580 voltage table.)

Schmitt Triggers should be used on the outputs of both the K580 and K581 when they are used for one shot or timer inputs.

Access to K580 and K581 inputs is by solder lugs only. Strain relief holes are provided in board (near handle) for a 9-wire cable. The avoidance of contact connectors on the logic wiring panel combined with heavy filtering guarantees noise isolation and protects modules by preventing accidental short circuits. Below is a summary of other characteristics.

| | Contact Current | Contact Voltage | Output for Contact Closed | Time Delay on Closure | Time Delay on Opening |
|---|---|---|---|---|---|
| K580 | 22ma | See Table | high | 10msec | 30msec |
| K581 | 22ma | 5V | low | 20msec | 20msec |

(Time delay figures above are nominal, and assume connection to the input of a standard gate such as K113 or K123.)

The contact current for the K581 comes from the logic supply, making it very important to assure freedom from accidental high voltages on K581 inputs, which could damage many logic modules by getting through to the system power supply. This hazard is not present with the K580, which uses an external source of +10 volts or more. The table below shows how external dropping resistors may be added to provide higher voltage operation.

**TABLE OF K580 VOLTAGE DROPPING RESISTANCES**

| CONTACT SUPPLY VOLTAGE | 10 | 12 | 15 | 24 | 28 | 48 | 90 | 100 | 120 |
|---|---|---|---|---|---|---|---|---|---|
| Dropping Resistance | 0 | 82Ω | 220Ω | 620Ω | 820Ω | 1.8KΩ | 3.6KΩ | 3.9KΩ | 4.7Ω |
| Dissipation | — | 0.05W | 0.11W | 0.3W | 0.4W | 0.85W | 1.8W | 2.0W | 2.5W |

When using dropping resistors and higher voltage supplies, total tolerance of resistors and supply should be ±10% to insure high levels between +4 V and +6 V at the logic. Also observe that a handful of dropping resistors in 90 V or 120 V systems may dissipate more power than the entire logic system, and must be located so as not to cause excessive temperature rise in the K series environment.

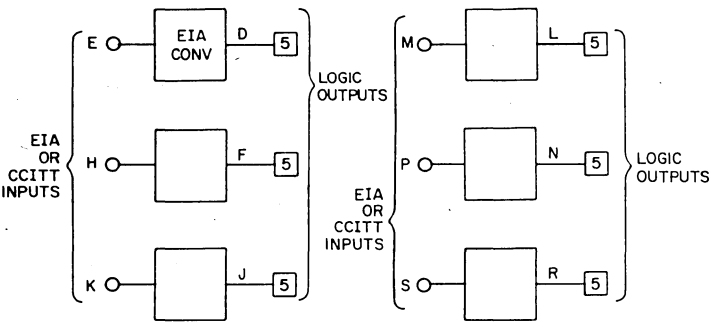
Note that these circuits may not be paralleled to obtain the wired OR or wired AND function, and that fanout is limited to 2 milliamperes in order to maintain the low (zero) output voltage within normal K-Series specifications. Fanout to ordinary logic gates and diode expanders may be raised to 4 milliamperes if some noise and contact bounce rejection can be traded off; but hysteresis inputs such as those at counter inputs, rate multiplier, etc., may not switch properly if the logic zero is allowed to rise much above +0.5 V.

Looking at the component side of both the K580 and K581, the solder lug connections are numbered 1 to 9 from pin end to handle end.

K580 — $28
K581 — $20

# EIA INPUT CONVERTER
K596

K SERIES




Any bipolar input signals with amplitudes between ±3 volts and ±25 volts will be transformed by this non-inverting converter into standard K-Series or M-Series logic signals with driving capabilities of 5 ma or 3 unit loads, respectively. Load for paralleling (wired OR): 1 milliampere. Input impedance stays between 3KΩ and 6KΩ for full capability with both the American EIA and the European CCITT standards for data transmission. Built-in noise filtering causes transition delays of several microseconds, limiting the maximum baud rate that can be handled.

Open-circuit inputs will produce low (zero-volts) outputs on the lower three circuits. The output stage of the first three circuits if inputs are open is controlled by pin B, which must be grounded for outputs low or connected to pin A (+5 volts) for outputs high. This last provision allows type 33 or type 35 current switching teletypes to be converted and wired ORed with modem interfaces. Pin B must be connected either to pin A or pin C: if it is left open, there may be crosstalk between circuits.

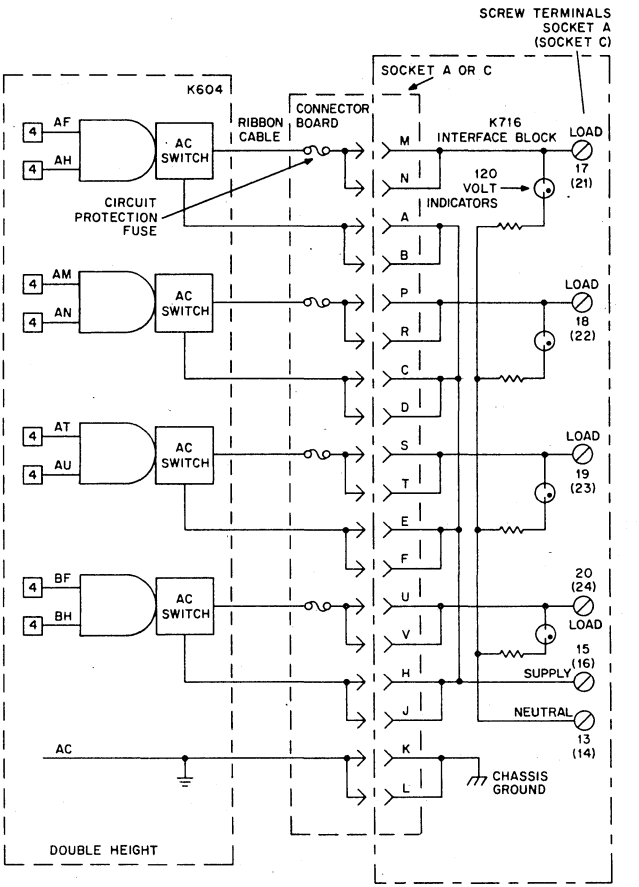
| Input | Pin B Connection | Pins D, F, J | Pins L, N, R |
|---|---|---|---|
| Open | C | 0 | 0 |
| Circuit | A | +5 | 0 |
| +3 to +25V | A or C | +5 | +5 |
| −3 to −25V | A or C | 0 | 0 |
| 0V | A or C | 0 | 0 |

Please observe that noise and interference can enter a digital system through any wires that pass through a noise field. K596 modules should be located at the edge of the system, and communication wiring should not be allowed to lie close to logic wiring for more than a few inches.

K596 — $20

# ISOLATED AC SWITCH
## K604

**K SERIES**




Operating in conjunction with the K782 or K716 Interface Block, the K604 permits AC operated valves, solenoids, small motors, motor starters and the like to be controlled directly from K Series logic. Each circuit can handle up to 250 volt-amperes continuously. Total for any module, however, should not exceed 500 volt-amperes averaged over one minute. Ratings below include maximum horsepower based on use of Allen-Bradley type K[R] motor starters. Less sensitive starters or relays may have significantly reduced capacity.

K604 — $110

| Maximum Capacity, each K604 circuit (120 v AC lines) | | | | | | |
|---|---|---|---|---|---|---|
| Condition | Continuous V.A. | Inrush V.A. | Motor Direct | Type K Starter | 208/220 Max. H.P. | 480/600 Max. H.P. |
| With Fuse | 250 | 600 | 1/20 H.P. | Size 3 | 30 | 50 |
| No Fuse | 250 | 1800 | 1/10 H.P. | Size 4 | 50 | 100 |

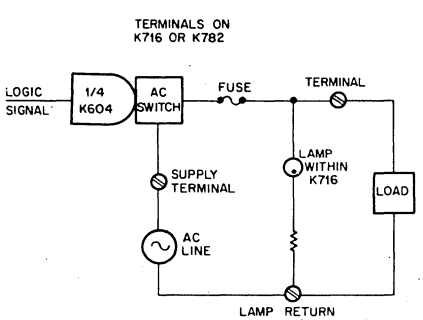
Littlefuse® type 275005 5 amp fuses provide fault protection for the triac output circuits. The fuses are mounted by clips on the connector board for easy replacement. Without the fuses, short circuits will destroy the module. The no-fuse information above is for reference only, and operation without fuse protection cannot be recommended. Circuits cannot be paralleled to increase ratings.

AC switch turnon takes place within 500 microseconds after input logic gate goes high. Turnoff takes place at zero crossings of the current. Maximum "off" leakage: 10 ma RMS at 140 VAC. Line voltage rating: 100 to 140 VAC, 50 to 60 Hz. Each triac output circuit has 400-volt breakdown rating. Shunt capacitor and shunt clipping devices inhibit false triggering on line transients.

Where very small devices such as pilot lamps, light duty relays, or AC input converters constitute the sole load, an auxiliary load such as a 12KΩ 2 watt resistor may be required to absorb sufficient holding current for full voltage output.

Two special precautions are made necessary by the presence of AC line voltages on the K604 module. First, always disconnect the ribbon cable connector before inserting or removing a K604 or an adjacent module, to avoid shocks or component damage. Second, W993 copper-clad boards ($4 each) should be installed between K604 modules and all other types except K508 or K644. **With the pin A connection cut away,** on either the board or the socket, the W993 copper clad board acts as an electrostatic shield. If this added interface protection is later found to be unnecessary, the sockets reserved for shield boards can be used to add logic features, modifications, etc. Refer to Construction Recommendations.

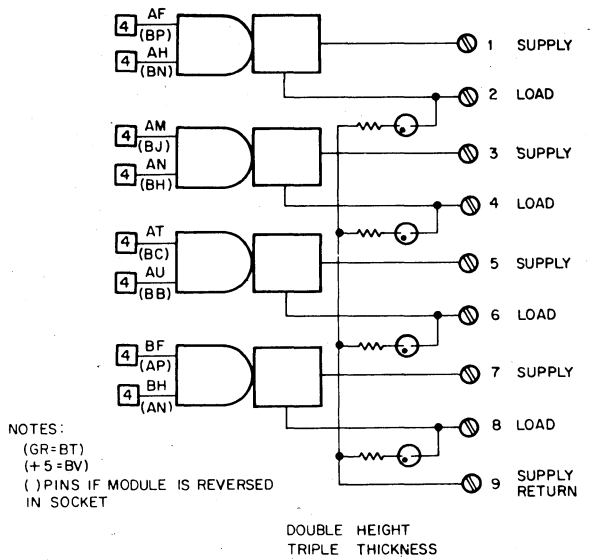
If desired, a K782 terminal board instead of the K716 may be used to obtain connections to field wiring. No indicators are provided by the K782, however.




K604 CIRCUIT IN USE

# ISOLATED AC SWITCH
## K614

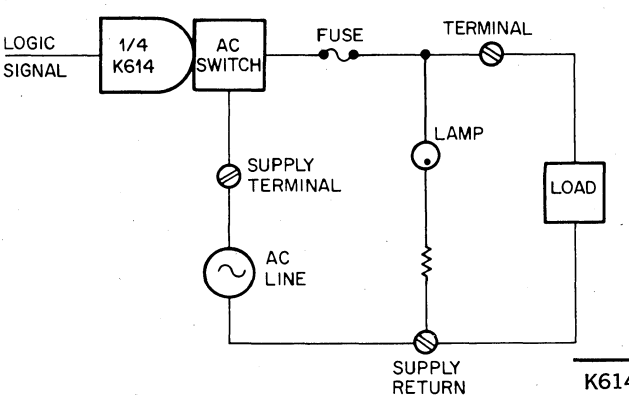
**K SERIES**




K614 AC SWITCH

This module uses the K604 circuit and behaves in most respects the same. However, the K614 is designed to fit a K724 interface shell. Accordingly the K614 has built-in clamp-type terminals for wires to size 14, interchangeable indicators, and output ratings boosted to 500 VA per circuit by the larger heat sink area available in this configuration.

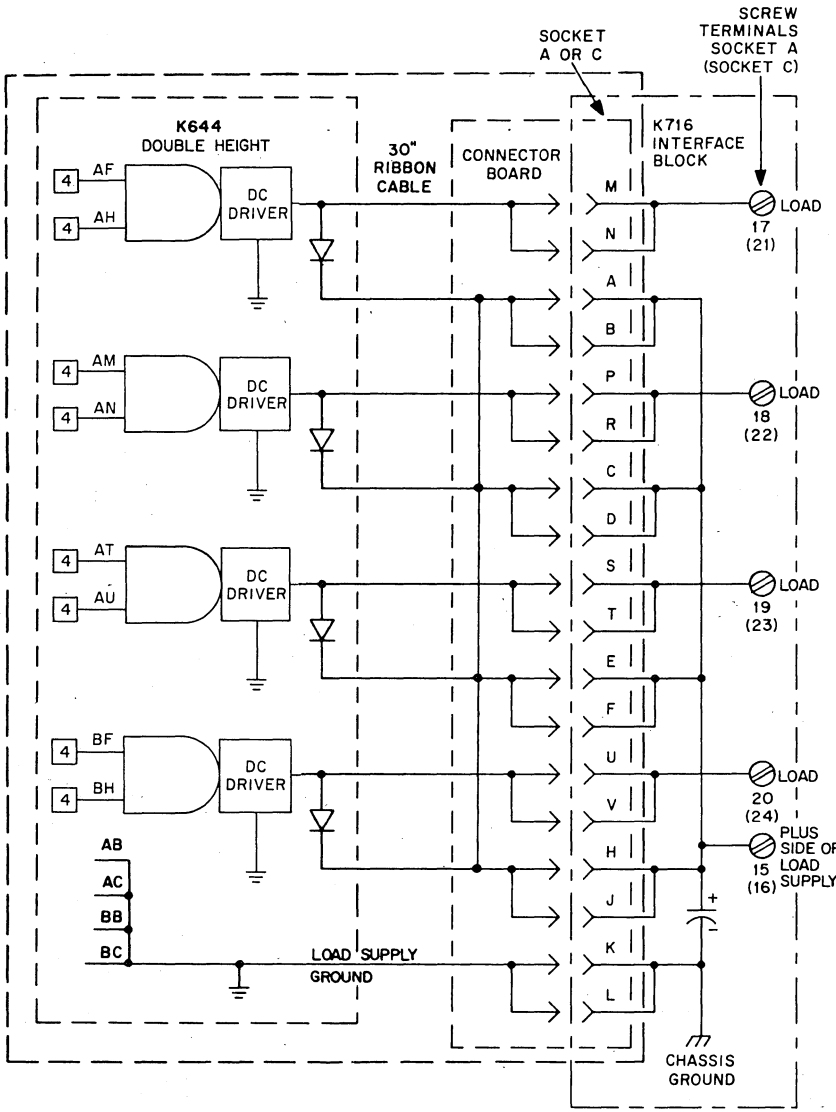
The outputs of the K614 are also fused for 5 amps like the K604.




K614 — $88

# DC DRIVER
K644

**K SERIES**



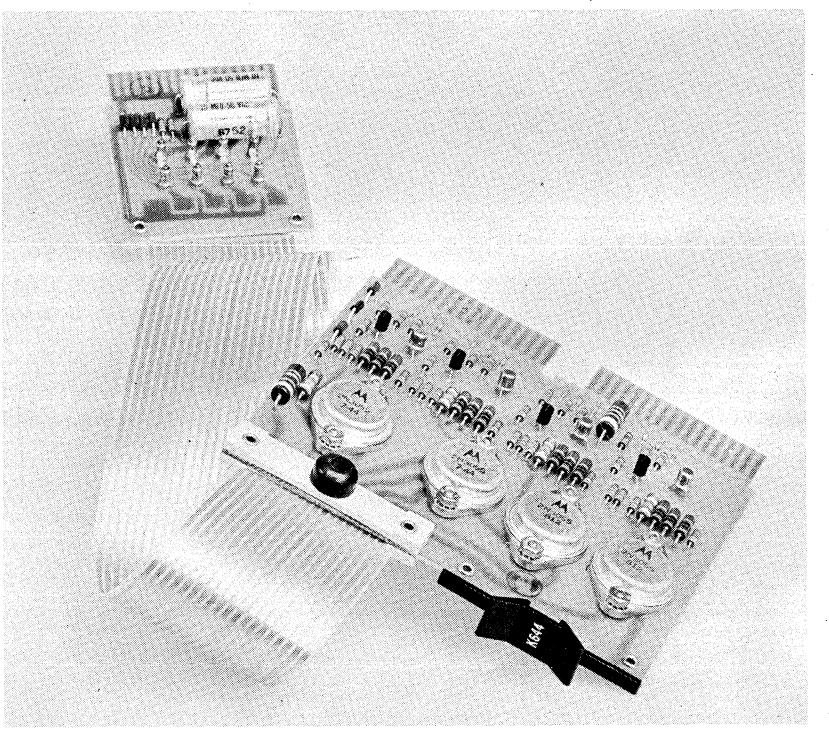

K644 — $66

Operating through the K782 or K716 Interface Block, the K644 DC Driver permits stepping motors, dc solenoids, and similar devices rated up to 2.5 amperes at 48 volts to be driven directly from K series logic. Built-in clamping diodes protect switching transistors from transient over-voltage.

Total output circuit current for the K644 module must not exceed 4 amperes averaged over any 1 minute period. The ribbon connector should be unplugged before inserting or removing a K644 module.

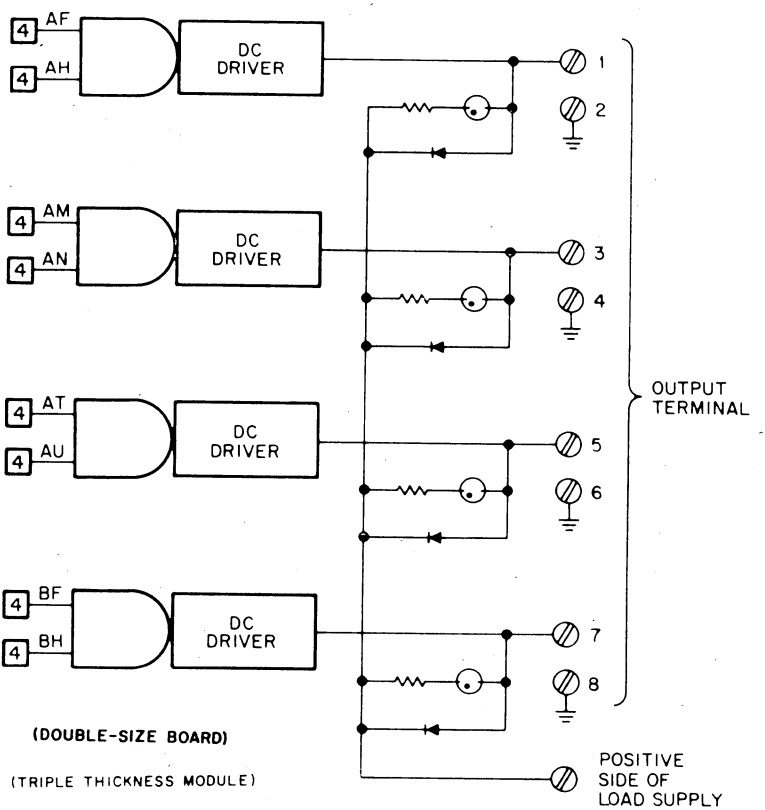
Moving the parts of a magnetic device change the winding inductance. To equalize magnetic field turnoff and turnon times, the ratio of inductance to total circuit resistance must be held constant. This demands more resistance in the circuit during turnoff, when the inductance is higher. Resistance may be inserted between K716 terminal 15 (or 16) and the load supply to achieve this, provided the K644 output voltage will not exceed 55 volts. Whether resistance is added or not, these clamp return terminals must be connected to the plus side of the load supply to protect the module from overvoltage during turnoff.

The K644 may be used with a K782 instead of a K716 to obtain the screw terminals needed for connecting heavy duty field wiring.



# DC DRIVER
K656

**K SERIES**



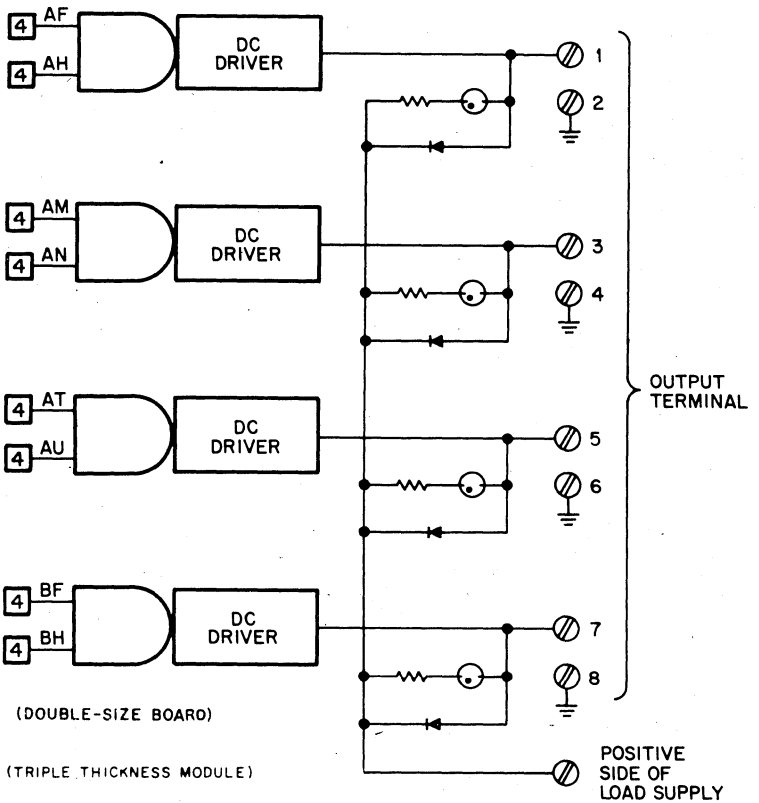

K656 250 VOLT DRIVER

Each circuit of this versatile driver can deliver up to 1 ampere at up to 250 volts, making it ideal for driving heavy-duty brakes and clutches or for high speed operation of other inductive loads. Like the K578 and K614, this module has integral clamp-type terminals and neon indicator lamps. (Lamps are effective only at 90 volts and above.) This driver module is designed to be used with K724 interface shells. Positive side of load supply must be connected to protect output transistors from damage during turnoff transient.

K656 — $80

# DC DRIVER
## K658

**K SERIES**



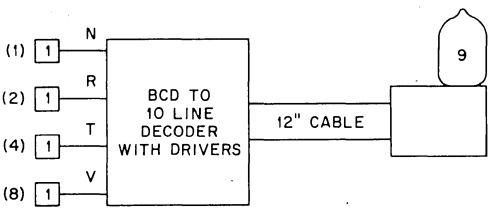

K658 4 AMP DRIVER

Each circuit of this versatile driver can deliver up to 4 amperes at up to 125 volts. Like the K578, K656 and K614, this module has integral clamp-type terminals and neon indicator lamps. (Lamps are effective only at 90 volts and above.) This driver module is designed to be used with K724 interface shells. Positive side of load supply must be connected to protect output transistors from damage during turnoff transient.

K658 — $128

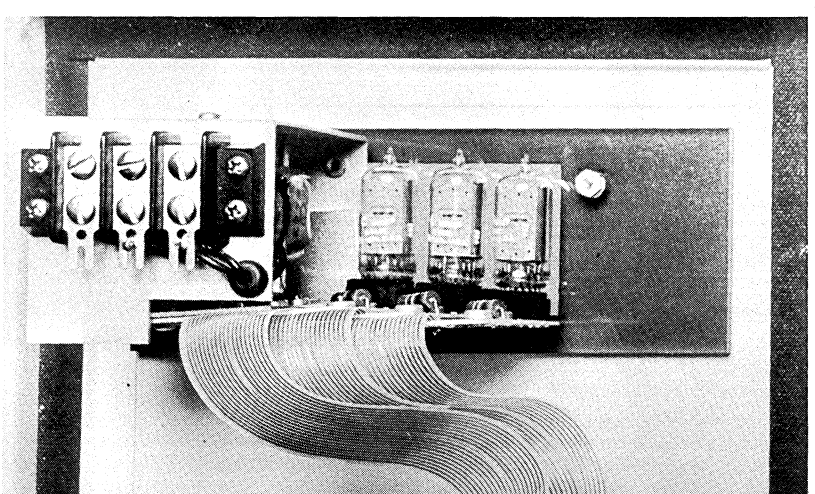
# DECIMAL DECODER AND NIXIE DISPLAY
K671

**K SERIES**



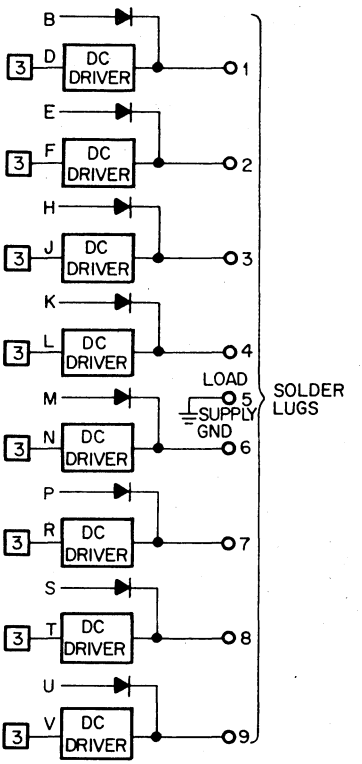

This module has two parts separated by a 1-foot ribbon cable. One part plugs into any module socket, the other contains a side-viewing Burroughs type B-5440 long life NIXIE glow tube on a mounting board. Four connections to corresponding module socket pins of a K210 or K220 binary-coded decimal counter completes the input wiring. The display tube board attaches with two screws to a K771 supply for both mechanical mounting and power supply electrical connections. Displays up to 6 digits long can be stacked on each K771 supply. Stacked digits have 0.8" mounting centers. See Construction Recommendations before assigning module locations. A Burroughs Type B-5442 NIXIE + and − glow tube can also be used in the K671. Ground pins N and V. Let pin R float and put input on pin T. Pin T is high for +, low for −.

K671 — $55

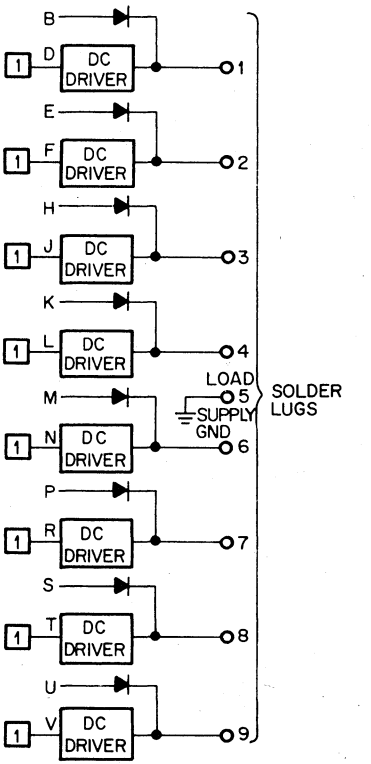


# LAMP DRIVERS
## K681, K683

**K SERIES**




K681 LAMP DRIVER



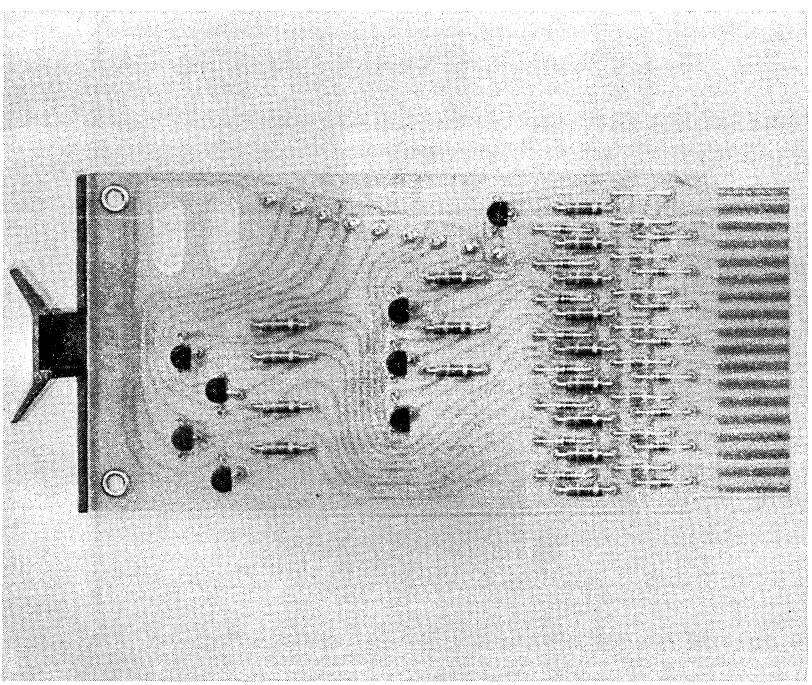

K683 LAMP DRIVER
(DOUBLE-SIZE BOARD)

These eight-circuit modules drive external loads through 9-conductor cable soldered to split lugs at the handle end by the user. Strain relief holes are prepunched in the board. Logic "0" turns the driver off, "1" turns it on.

Pin connections via diodes to outputs facilitate production automatic module testing while isolating system wiring from high voltages. Circuits are not slowed, and these connections are not recommended as output tiepoints unless exceptional care is taken to prevent noise and damaging voltages from degrading system reliability.

| MODULE TYPE | OUTPUT RATINGS | | |
|---|---|---|---|
| | RESISTIVE | INDUCTIVE | INCANDESCENT LAMPS |
| K681 | 18V, 30ma | 18V, 30ma with added suppression diodes (K784) | Lamps rated 18V, 40ma operated at 12V to reduce current to 30 milliamperes |
| K683 | 55V, 250ma | 55V, 250ma with added suppression diodes (K784) | Lamps rated 40ma, to 48V; Lamps rated 60ma, to 28V; Lamps rated 80ma, to 18V; Lamps rated 100ma, to 12V |

Note greatly reduced ratings on tungsten loads. Lamp filaments draw typically ten times more current at turnon than when hot, resulting in very high transistor dissipation if supply voltage is high. Series current limiting resistors or shunt preheat resistors could be used to limit surge in certain cases, but ratings above assume this would be awkward or impractical.



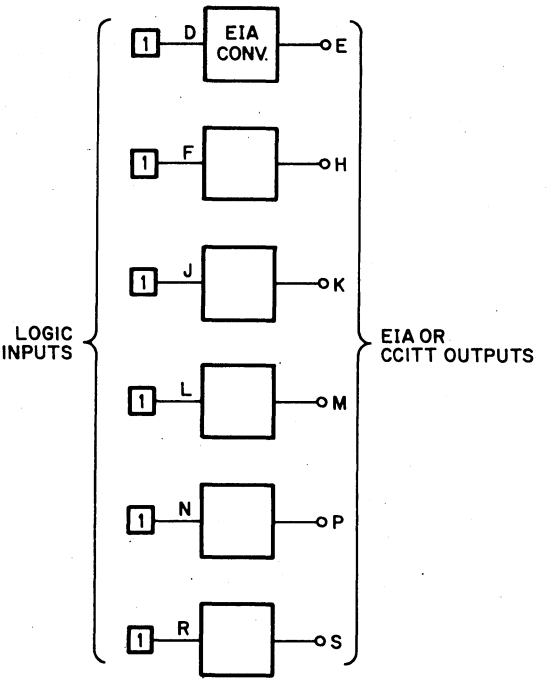
K681

Solder lugs on both the K681 and K683 shown above are numbered 1 to 9 from left to right.

K681 — $15
K683 — $30

# EIA OUTPUT CONVERTER
K696

**K SERIES**




EIA OUTPUT CONVERTER K696

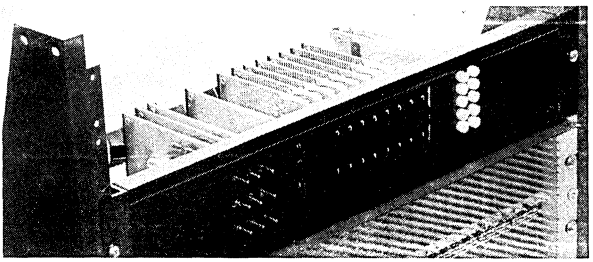
This bipolar non-inverting driver converts standard logic levels to either the American EIA or the European CCITT standard signals for data transmission. Power can either be 6.3 VAC±10% 60Hz on pin B for EIA levels (at least ±5 volts) or 9.0 VAC±10% 50Hz on pin B for CCITT levels (at least ±6 volts). Limited output current capability results in risetimes of several microseconds for capacitive loads of a few thousand picofarads, limiting the maximum baud rate to 5K baud. One ampere of AC can supply up to 32 K696 modules. Keep AC leads short to maintain voltage.

Please observe that noise and interference can enter a digital system through any wires that pass through a noise field. K696 modules should be located at the edge of the system, and communications wiring should not be allowed to lie close to logic wiring for more than a few inches. A high impedance probe may be used to monitor the half-wave rectified and filtered negative internal supply at pin T (5 KΩ series resistance).

K696 — $44

# MODULAR PANEL HARDWARE
## K950

K SERIES



The K950 Magnetic modular panel hardware provides a convenient way to build control panels containing lights, toggle and push button switches, timer controls, and thumbwheel switches. The lower connector half of the control modules K410, K420, K422, K424, and K432 are plugged into the upper connectors across a K943 mounting panel and the manual controls protrude through the K950 panel frame. The K410, K420, and K432 modules are supplied with a precut panel piece that fills the panel space for the module. The K422 and K424 modules do not require a panel piece. Since each module is covered independently of the next module, any module type can be plugged into any one of the available 32 panel socket locations. All panel hardware is supplied painted black, however, panel pieces may be individually repainted to give color coded meaning to panel controls. Thumbwheel modules are black plastic and can not be painted.

A control module can be inserted into any socket except the one directly to the left of a K422 or K424 thumbwheel module. For this reason it is recommended that all thumbwheel registers be grouped together in the same section of the panel to conserve panel locations. Metal spacers of single or double module width are available to cover unused panel locations.

The frame and panel pieces are made of steel and are held together with rivets and flexible strip magnets. The frame is mounted in a standard 19 inch rack directly above a socket mounting panel. After the control modules have been inserted into their chosen socket locations, the steel panel pieces are snapped into place to cover the modules and unused loactions. After the panel is completely filled, a steel bezel is snapped into place over the panel pieces and the panel is complete.

The panel hardware can be disassembled at any time to allow controls to be added or removed.

When the panel is completely assembled, most of the magnetic lines of force are closed through the steel panel pieces. However, steel dust particles and filings will still be attracted to the panel surfaces. The magnetic force from the panel is not strong enough to damage a watch worn by the user. Each K950 is supplied with 8 single and 8 double spacers to cover up to 24 unused panel locations. The K950 is 3½ inches in height.

K950 — $39.

The Module Assembly area has shifted emphasis from volume production to complex experimental work. The above process is a special sub-assembly of an indicator light board designed for a control unit.

# A SERIES

# NOTES ON OPERATIONAL AMPLIFIERS

## I. INTRODUCTION

This article describes some of the basic characteristics and uses of operational amplifiers. It is written especially for people with a digital background, but with a limited exposure to analog technology. The equations presented are not exact, but are good engineering approximations, which are accurate enough for most applications. It is hoped that this simplified discussion will provide more insight into the uses and limitations of operational amplifiers than a more rigorous approach.

The operational amplifier is a basic building block in analog work, much the same way as a NAND gate can be a basic building block in a digital computer. An operational amplifier (op amp) together with other components such as resistors and capacitors, can be used to perform addition, subtraction, integration, and many other functions. Op amps can be used to make oscillators, active filters, and even digital circuits such as Schmitt triggers, gates, and flip-flops. When used with A/D and D/A converters in data processing work, op amps perform such functions as scale changing, offsetting, and isolation between source and load.

## II. GENERAL CHARACTERISTICS

An operational amplifier can be considered a 3 terminal device, plus a common or ground return, see Fig. 1. Chopper-stabilized op amps, which will not be considered here, have the Plus Input permanently tied to ground. The op amp is really a difference amplifier, in that it amplifies only the difference between the two inputs, and tries to reject any DC or AC signal that is common to both inputs.

Op amps are characterized by high DC gain, high input impedance, low output impedance, and a gain that decreases with increasing frequency. Op amps used without feedback would be operating open loop, a rare situation; but with feedback the operation would be closed loop. The use of properly applied negative feedback stabilizes the operation of the composite circuit against changes in the amplifier, and provides its versatility and usefullness.

When an op amp is working in the linear region, two approximations can be made to help in the analysis of the circuit configuration. First, the voltages of the two inputs are the same; and second, no current flows into or out of the input terminals. Fig. 2 shows a simple inverting amplifier. Assume the Minus Input is 0 volts, the same as the Plus Input, and that no current flows into the Minus Input, called the summing junction. Then $i_I = i_F$, and some simple manipulations show that the gain is equal to $-R_F/R_I$. Similar reasoning applied to the non-inverting amplifier of Fig. 3 shows that the gain is equal to $+\frac{R_1 + R_2}{R_1}$. An easy way to remember this is to think of the two resistors as forming a tapped divider network.

## III. SPECIFICATIONS

Specifications are usually given for open loop performance, so that the user has to interpret and calculate how this will affect his particular closed loop circuit. The following section will give some brief descriptions of what some of the specifications mean.

**Settling time.** This is the time it takes the output to get within and stay within a certain amount of is final value, after the input has received a step input, see Fig. 4. This parameter is important when an amplifier is used in front of an A/D converter, since the A/D should not begin its conversion until the amplifier has settled.

**Overload recovery.** It takes an overload recovery time for the output to first assume its proper value after an overdriving input signal has been removed. However, the output still has not settled, and this extra time must be waited before the output is valid.

**Slew rate.** This term is comparable to rise or fall time in a digital circuit. It is a measure of how fast the output can change. If an amplifier output could go from 0 volts to 10 volts in 2 μsec, it would have a slew rate of 5 volts/μsec.

**Frequency for full output.** This is the maximum frequency at which a full scale sine wave (such as +10 to −10 volts) can be assured at the output, without noticeable distortion. In many ways this is real frequency limitation of an op amp, since up to this frequency there are no other restrictions on the amplitude of the input signal.

**Frequency for unity gain.** The open loop gain of an amplifier is equal to one at this frequency. But the input signal must be restricted in amplitude such that the maximum rate of change of output (slew rate) is not exceeded. Usually only millivolt signals may be processed at this frequency, therefore the full amplifier bandwidth is not usable for normal data processing systems.

**Impedance.** The input impedance is simply the resistance between the two inputs. The common mode impedance is the highest resistance attainable with feedback.

**Common mode rejection.** This is a measure of how well an amplifier will not respond to a signal common to both inputs. If used as a voltage follower, an op amp with a common mode rejection ratio (CMRR) of 10,000 could have error of 1 mv if the input were 10 v. (10/10,000 volts).

**Voltage offset.** The inability to achieve perfect balance in the input circuit causes the output to respond to an apparent signal when the inputs are tied to ground. For an inverting amplifier, the output error due to the input voltage offset is equal to the offset times the closed loop gain plus one. With an input offset of 3 mv, and a gain of 1, the output error would be 6 mv. Fortunately, initial voltage offset can be trimmed with a potentiometer at the right place in the circuit.

**Current offset.** Current offset (or bias current) multiplied by the feedback resistor (Fig. 2) produces an output error. This effect can be minimized by using the differential offset (the difference in offset currents for the two inputs) when the resistance seen from both inputs to ground are equal. For Fig. 2, the Plus Input should than be returned to ground through a resistor equal to the parallel combination of $R_I$ and $R_F$.

**Output ratings.** The output voltage and current ratings imply a minimum value for the load resistor. 10 volts and 5 ma would correspond to a load resistor of 2 K. In an inverting amplifier, the feedback resistor is a load for the output, and the current through this resistor must be subtracted from

the amount of current still available at the output. All really useful operational amplifiers can be shorted to ground without damage, but shorting to a voltage will usually destroy some of the circuitry.

## IV. APPLICATIONS

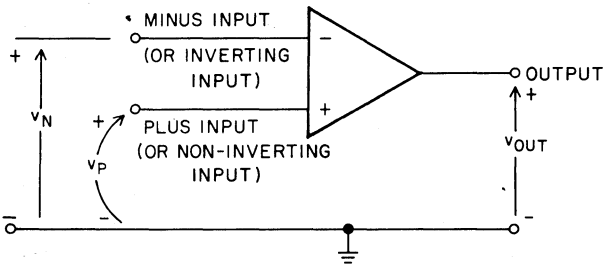
Some common configurations for operational amplifiers are shown in Figs. 5 through 10. The pin letter assignments correspond to the op amps sold by Digital Equipment Corp. If these op amps are used, the jumper between Pin S and the Minus inpunt should be removed.

The voltage follower, Fig. 5, features high input impedance, but will have an error depending on the CMRR. Large voltages cannot be handled, since common mode voltage ratings should not be exceeded. The inverter configuration, Fig. 7, is very versatile and does not have a common mode voltage problem, since both inputs are near ground. Large input voltages can be handled if the input resistor is made appropriately large. One disadvantage of the inverting configuration is that the input impedance is relatively low, essentially equal to the input resistor. When a gain trim potentiometer is used, the gain accuracy by itself becomes irrelevant. What is important is gain resolution (mostly determined by the potentiometer), and the gain stability (mostly determined by the temperature coefficients of the input and feedback resistors). The ratio of the closed loop gain to the open loop gain gives the suitability of an amplifier as far as static accuracy is concerned. With a closed loop gain of 5, and an open loop gain of 10,000, an amplifier could be used in a system with an allowable error of 1 part in 2,000.

The possibility of oscillation must always be considered when feedback amplifiers are used. Usually the more feedback used, the greater is the tendency to oscillate. Oscillations can always be attributed to phase shift. Therefore, stabilization of operational amplifiers involves phase shifting to oppose oscillation. In Fig. 7, the feedback capacitor allows high frequency signals to be fed back to the inverting input (degenerative feedback) with a phase lead. In the inverting configuration, the output will be 180° out of phase with the input at low frequencies, and the feedback signal will oppose the input signal. At high frequencies, these are additional phase lags in the amplifier and feedback circuitry. If the feedback signal has a total phase shift (lag) of 360° with a gain through the amplifier and feedback network of greater than 1, the amplifier will oscillate, since the input and output are in phase.

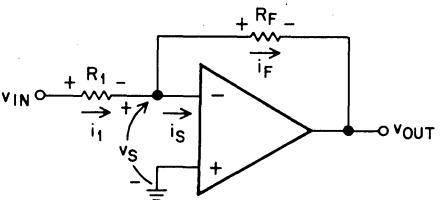
## V. REFERENCES


1. "An Operational Amplifier Application Manual"
   Analog Devices, Inc., Cambridge, Mass.
2. "Handbook of Operational Amplifier Applications"
   Burr-Brown Research Corp., Tucson, Arizona
3. "Linear Integrated Circuits Applications Handbook"
   Fairchild Semiconductor, Mountain View, California
4. "Applications Manual for Operational Amplifiers"
   Philbrick/Nexus Research, Dedham, Mass.




$v_{OUT} = A(v_P - v_N)$, WHERE A IS THE AMPLIFIER GAIN

Fig. 1, Basic Operational Amplifier Symbol



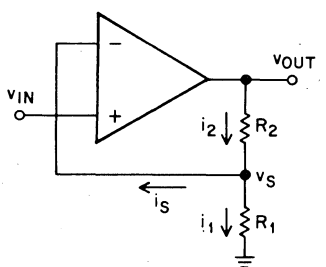

ASSUME: $v_S = 0$ THEN $i_1 = i_F$

$i_S = 0$

$$\frac{v_{IN}}{R_1} = -\frac{v_{OUT}}{R_F}$$

$$\frac{v_{OUT}}{v_{IN}} = -\frac{R_F}{R_1}$$

Fig. 2, Inverting Amplifier




ASSUME: $v_S = v_{IN}$

$i_S = 0$

THEN $i_1 = i_2$

$$\frac{v_S}{R_1} = \frac{v_{OUT} - v_S}{R_2}$$

$$\frac{v_{IN}}{R_1} = \frac{v_{OUT} - v_{IN}}{R_2}$$

$$v_{IN} R_2 = v_{OUT} R_1 - v_{IN} R_1$$

$$\frac{v_{OUT}}{v_{IN}} = +\frac{R_2 + R_1}{R_1}$$

Fig. 3, Non-Inverting Amplifier

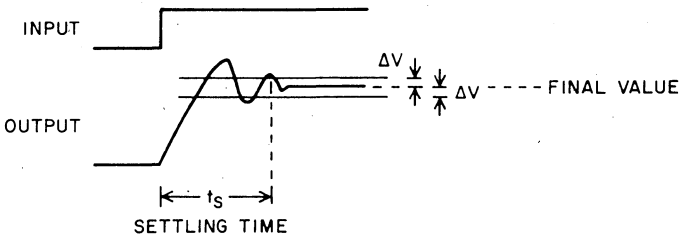



Fig. 4, Setting Time

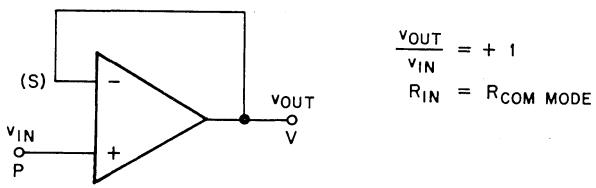



Fig. 5, Voltage Follower

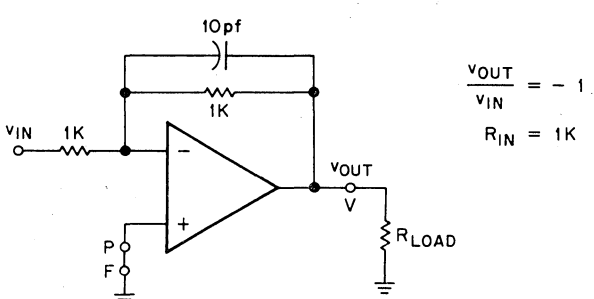
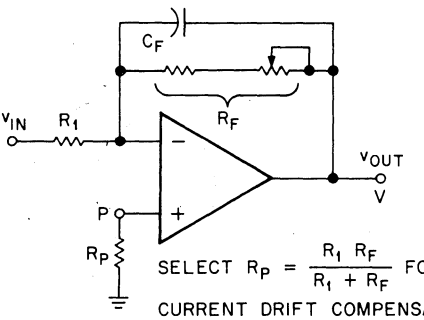



Fig. 6, Inverter




$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_1}$$

$R_{IN} = R_1$

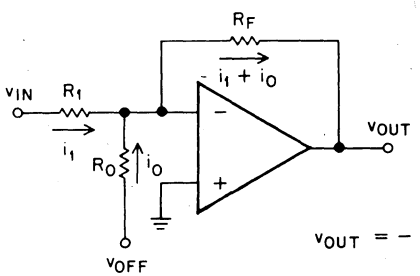
GAIN STABILITY DEPENDS ON THE INPUT AND FEEDBACK RESISTOR, AND GAIN TRIM POTENTIOMETER.

TYP VALUES

| | |
|---|---|
| $R_1$ | 1K TO 10K |
| $R_F$ | 1K TO 100K |
| $R_P$ | 500Ω TO 5K |

THE USE OF $C_F$ REDUCES THE TENDENCY OF THE OP AMP TO OSCILLATE

Fig. 7, Adjustable Gain and Current Compensation




$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_1}\right) + \underbrace{\left[-V_{OFF}\left(\frac{R_F}{R_O}\right)\right]}_{\text{OFFSET}}$$

Fig. 8, Offsetting

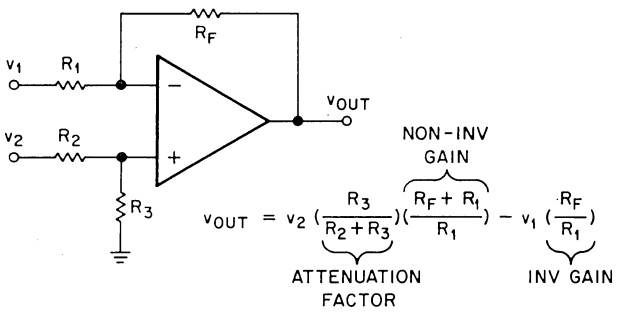
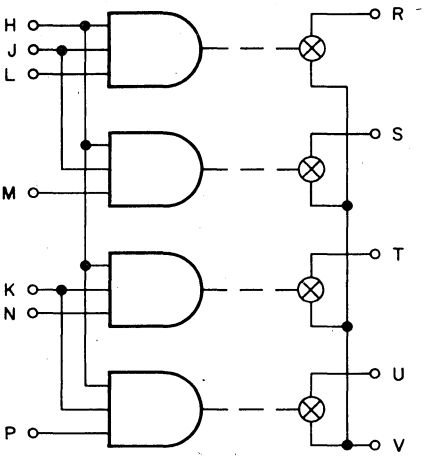



Fig. 9, Differential Gain

# POSITIVE LOGIC MULTIPLEXER
A123

**A SERIES**




| INPUT | OUTPUT TERMINALS |
|---|---|
| +3V | CONNECTED |
| 0V | OPEN |

The A123 Multiplexer provides 4 gated analog switches that are controlled by logic levels of 0v and +3v. The module is equivalent to a single-pole, 4-position switch, since one output terminal of each MOS FET switch is tied together. If all three digital inputs of a circuit are at +3v (or not connected) the two output terminals are connected together. If any digital input is at 0v, the switch terminals are disconnected. Two switches should not be on at the same time. The analog switch can handle signals between +10v and −10v, with currents up to 1 ma.

The positive power supply must be between +5v and +15v, and at least equal to or greater than the most positive excursion of the analog signal. The negative power supply must be between −5 and −20v, and at least 10 volts more negative than the most negative excursion of the analog signal. The voltage difference between the two supplies must not be more than 30v.

## SPECIFICATIONS

**Digital Inputs**

| | |
|---|---|
| Logic ONE: | +2.4v to +5.0v |
| Logic ZERO: | 0.0v to +0.8v |
| Input loading: | 0.5 ma at 0 volts |

**Analog Signal**

| | |
|---|---|
| Voltage range: | +10v to −10v |
| Current (max.): | 1 ma |

**Output Switch**

| | |
|---|---|
| On resistance, max.: | 1000 ohms |
| On offset: | 0 volts |
| Off leakage, capacitance: | 10 na, 10 pf |
| Turn on delay, max.: | 0.2 μsec |
| Turn off delay, max.: | 0.5 μsec |

**Power**

| | |
|---|---|
| +5v (pin A): | 45 ma |
| +v (pin D): | 18 ma (for +10v) |
| −v (pin E): | 50 ma (for −20v) |

A123—$58

# OPERATIONAL AMPLIFIER
## A200

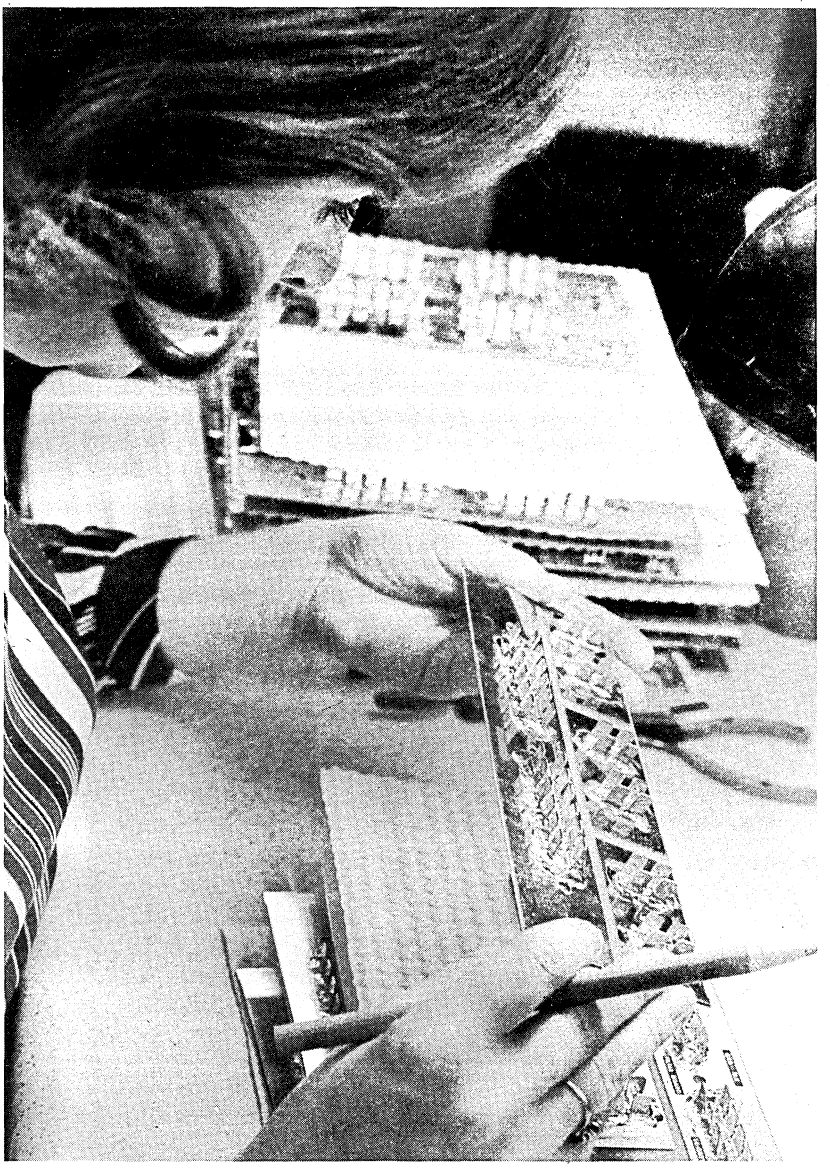
**A SERIES**

The A200 is an operational amplifier mounted on an A990 amplifier board. Provisions are made on the board for the mounting of potentiometers for gain trim and balance. Mounting holes are also provided for input and feedback networks, and rolloff capacitor. The module is a double width board.

| | |
|---|---|
| OPEN LOOP GAIN: | $2x10^6$ |
| RATED OUTPUT | |
| Voltage: | ±11v |
| Current: | 20 ma |
| FREQUENCY RESPONSE | |
| Unity gain, small signal: | 10 MHz |
| Full output voltage: | 300 kHz |
| Slewing rate: | 30v/μsec |
| Overload recovery: | 200 μsec |
| INPUT VOLTAGE OFFSET (Adjustable to Zero) | |
| Average vs. Temperature: | 20 μv/°C |
| Average vs. Supply voltage: | 15 μv/% |
| Average vs. Time: | 10 μv/day |
| INPUT CURRENT OFFSET: | ±2 na |
| Average vs. Temperature: | 0.4 na/°C |
| Average vs. Supply voltage: | 0.15 na/% |
| INPUT IMPEDANCE | |
| Between inputs: | 6 megohm |
| Common mode: | 500 megohm |
| INPUT VOLTAGE | |
| Maximum: | ±15 volts |
| Maximum common mode: | ±10 volts |
| Common mode rejection: | 20,000 |
| POWER | |
| Voltage: | ±15 volts |
| Current at rated load: | 35 ma |

*REFER TO A990 FOR CONNECTIONS

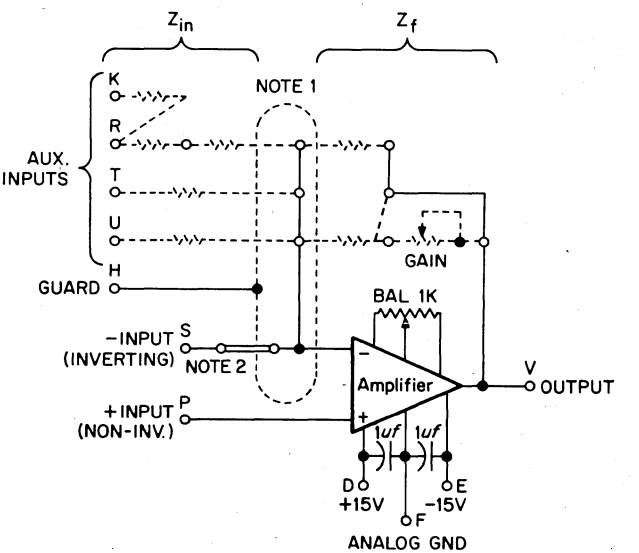
A200 — $130



After the modules are flow-soldered, they undergo a visual inspection to insure that all solder points and runs are properly made. If needed, additional solder is added.

# OPERATIONAL AMPLIFIER
## A206

**A SERIES**




NOTE 1. Mounting holes are provided on the module so that input and feedback components can be added. Components shown with dashed lines are not included with the module.

NOTE 2. This jumper comes with the module. It may be removed to suit circuit requirements.

The A206 Operational Amplifier features extremely fast settling time (2 μs to within 1 mv), making it especially suited for use with Analog-to-Digital Converters. FET's are used in the input stage to provide high input impedance. The A206 can be used for buffering, scale-changing, offsetting, and other data-conditioning functions required with A/D converters. All other normal operational amplifier configurations can be achieved with the A206.

The A206 is supplied with a zero balance potentiometer. Provisions are made on the board for the mounting of input and feedback components, including a gain trim potentiometer. The A206 is pin-compatible with the A200 Operational Amplifier.

**SPECIFICATIONS**—At 25°C, unless noted otherwise.

| | |
|---|---|
| **Settling Time*** | |
| Within 1 mv, 10v step input, typ: | 1.5 μsec |
| Within 1 mv, 10v step input, max: | 2.0 μsec |
| **Frequency Response** | |
| DC open loop gain, 670 ohm load, min: | 100,000 |
| Unity gain, small signal, min: | 10 MHz |
| Full output voltage, min: | 1 MHz |
| Slewing rate, min: | 100v/μsec |
| Overload recovery, max: | 0.5 μsec |
| **Output** | |
| Voltage, max: | ±10v |
| Current, max: | ±15 ma |
| **Input Voltage** | |
| Input voltage range, max: | ±10v |
| Differential voltage, max: | ±15v |
| Common mode rejection, min: | 7,000 |
| **Input Impedance** | |
| Between inputs, min: | $10^{10}$ ohms |
| Common mode, min: | $10^{10}$ ohms |
| **Input Offset** | |
| Avg. voltage drift vs. temp., max: | ±30 μv/°C |
| Avg. volt. drift vs. supply volt., max: | ±20 μv/% |
| Initial differential current offset, max: | 0.03 na |
| Avg. dif. cur. drift vs. temp., max: | ±0.003 na/°C |
| **Temperature Range** | 0°C to +60°C |
| **Power** | |
| +15v (pin D), quiescent: | 15 ma |
| −15v (pin E), quiescent: | 15 ma |

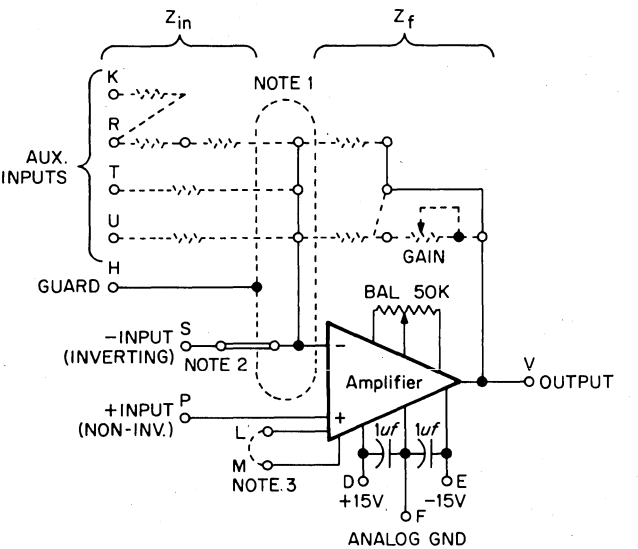
If the Output is accidentally shorted to ground, the amplifier will not be damaged.

*Gain of 1, inverting or non-inverting configuration.

A206 — $190

# OPERATIONAL AMPLIFIER
## A207

**A SERIES**




NOTE 1. Mounting holes are provided on the module so that input and feedback components can be added. Components shown with dashed lines are not included with the module.

NOTE 2. This jumper comes with the module. It may be removed to suit circuit requirements.

NOTE 3. Pins L & M can be connected together to improve settling time, but parameters such as drift and open loop gain are degraded.

The A207 is an economical Operational Amplifier featuring fast settling time (5 μs to within 10 mv), making it especially suited for use with Analog-to-Digital Converters. The A207 can be used for buffering, scale-changing, offsetting, and other data-conditioning functions required with A/D Converters. All other normal operational amplifier configurations can be achieved with the A207.

The A207 is supplied with a zero balance potentiometer. Provisions are made on the board for the mounting of input and feedback components, including a gain trim potentiometer. The A207 is pin-compatible with the A200 Operational Amplifier.

**SPECIFICATIONS**—At 25°C, unless noted otherwise.

| | Pins L & M Connected | Differences with Pins L & M Not Connected |
|---|---|---|
| **Settling Time*** | | |
| Within 10 mv, 10v step input, typ: | 3 μsec | 6 μsec |
| Within 10 mv, 10v step input, max: | 5 μsec | 8 μsec |
| Within 1 mv, 10v step input, max: | 7 μsec | 10 μsec |
| **Frequency Response** | | |
| DC open loop gain, 670 ohm load, min: | 15,000 | 100,000 |
| Unity gain, small signal, min: | 3 MHz | |
| Full output voltage, min: | 50 KHz | |
| Slewing rate, min: | 3.5v/μsec | |
| Overload recovery, max: | 8 μsec | |
| **Output** | | |
| Voltage, max: | ±10v | |
| Current, max: | ±15 ma | |
| **Input Voltage** | | |
| Input voltage range, max: | ±10v | |
| Differential voltage, max: | ±10v | |
| Common mode rejection, min: | 10,000 | |
| **Input Impedance** | | |
| Between inputs, min: | 100 K ohms | |
| Common mode, min: | 5 M ohms | |
| **Input Offset** | | |
| Avg. voltage drift vs. temp, max: | 60 μv/°C | 30 μv/°C |
| Initial current offset, max: | 0.5 μa | |
| Avg. current drift vs. temp, max: | 5 na/°C | |
| **Temperature Range** | 0°C to +60°C | |
| **Power** | | |
| +15v (pin D), quiescent: | 6 ma | |
| −15v (pin E), quiescent: | 10 ma | |

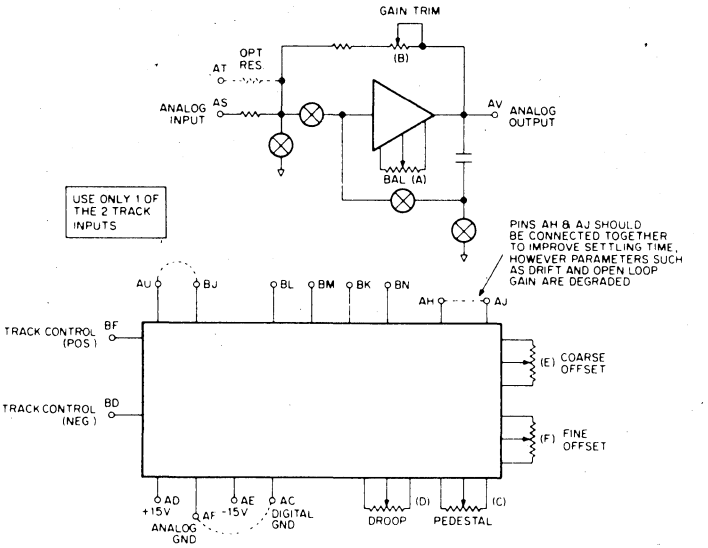
If the Output is accidentally shorted to ground, the amplifier will not be damaged.

*Gain of 1, inverting or non-inverting configuration.

A207 — $45

# SAMPLE AND HOLD
## A404

**A SERIES**




JUMPER CONNECTIONS TO OFFSET OUTPUT

| | MODE | |
|---|---|---|
| PIN | TRACK (sample) | HOLD |
| BF (pos) | +3v or open | 0v |
| BD (neg) | −3v or open | 0v |

| Positive | Negative |
|---|---|
| AU to BJ | AU to BJ |
| | BL to AD |
| BM to AE | |
| BK to AF | BN to AF |

Analog gnd (pin AF) and digital gnd (pin AC) must be connected together at one point in the system.

The A404 Sample & Hold has an acquisition time of 6 μsec for a 10 volt signal to within 10 mv (0.1%). The circuit inverts the input signal, and has an input impedance of 10 K. Features of the circuit include potentiometers to control the pedestal and the droop of the output signal.

Two digital Track Control (sample) inputs are provided: one for negative logic (0v & −3v), and the other for positive logic (0v & +3v). Either input by itself will perform the necessary control, and the inadvertent application of both digital signals will cause no damage to the circuit.

Potentiometers are also provided for zero balancing, gain trim, and offset adjustment (up to ±10v). If offsetting is desired, connections should be made according to the table shown with the diagram. The A404 is pin-compatible with the A400 Sample & Hold.

**SPECIFICATIONS**—At 25°C, unless noted otherwise. Pins AH & AJ are connected together.

**Acquisition Time**

| | |
|---|---|
| Within 10 mv, 10v step input, typ: | 4 μsec |
| Within 10 mv, 10v step input, max: | 6 μsec |
| Within 2.5 mv, 10v step input, max: | 11 μsec |

**Aperture Time,** max: 0.2 μsec

**Gain** —1.000 (adjustable ±0.2%)

**Input**

| | |
|---|---|
| Voltage range, max: | ±10v |
| Impedance: | 10 K ohms |

**Output**

| | |
|---|---|
| Voltage range, max: | ±10v |
| Current, max: | 10 ma |

**Pedestal***

| | |
|---|---|
| Initial pedestal: | Adjustable to less than 1 mv |
| Pedestal variation vs. temp, max: | 0.2 mv/°C |

**Droop**

| | |
|---|---|
| Initial droop: | Adjustable to less than 5 mv/ms |
| Droop variation vs. temp, max: | 2 mv/ms/°C |

**Track Control**

| | |
|---|---|
| Pos. (pin BF) | +3v, Track<br>0v at 2 ma, Hold |
| Neg. (pin BD) | —3v, Track<br>0v at 1 ma, Hold |

**Board Size** 1 double height board, single module width

**Temperature Range** 0°C to +50°C

**Power**

| | |
|---|---|
| +15v (pin AD), quiescent: | 22 ma |
| —15v (pin AE), quiescent: | 35 ma |

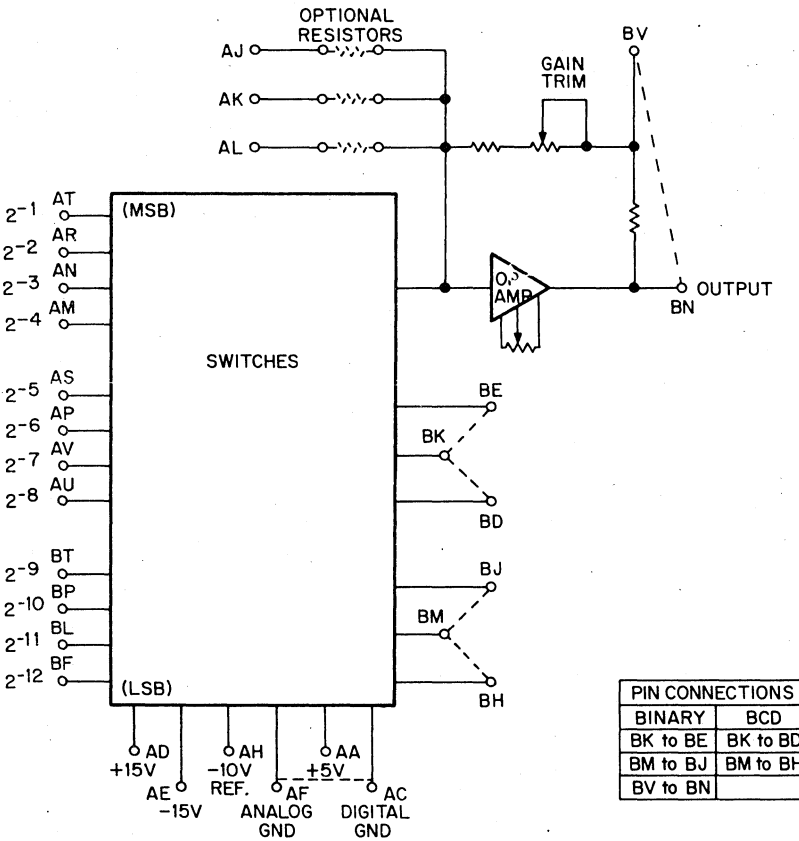
If the Output is accidentally shorted to Ground, the circuit will not be damaged.

*Difference in output voltage when changing from Track to Hold mode.

A404 — $130

# 12-BIT DAC
A613

**A SERIES**




| PIN CONNECTIONS | |
|---|---|
| BINARY | BCD |
| BK to BE | BK to BD |
| BM to BJ | BM to BH |
| BV to BN | |

| BINARY INPUTS | | OUTPUT |
|---|---|---|
| $2^{-1}$ | ALL OTHERS | |
| 0V | 0V | +0.000V |
| +3 | 0 | +5.000 |
| +3 | +3 | +9.9975 |

ANALOG GND (PIN AF) & DIGITAL GND (PIN AC) MUST BE CONNECTED TOGETHER AT ONE POINT IN THE SYSTEM.

The A613 is a 12-bit Digital-to-Analog Converter for moderate speed applications. The module is controlled by standard positive logic levels, has an output between 0v and +10v, and will settle within 50 μsec for a full scale input change. The input coding can be either straight binary or 3 decades of 8421 BCD with only simple connector jumpers required to take care of the change.

The A613 requires a −10.0v reference that can supply negative current, such as an A704. Provisions are made for adding up to 3 extra resistors to implement offsetting functions. Potentiometers are provided for zero balancing, and gain trim. The A613 is a double height board.

An input of all Logic 0's produces zero volts out; all Logic 1's produces close to +10v out. The operational amplifier output can be shorted to Ground without damaging the circuit.

## SPECIFICATIONS

**Inputs**

| | |
|---|---|
| Logic ONE: | +2.0v to +5.0v |
| Logic ZERO: | 0.0v to +0.8v |
| Input loading: | 1 ma (max.) at 0 volts |

**Output**

| | |
|---|---|
| Standard: | 0v to +10v |
| Optional, (requires Positive REF) | 10v range between −10v and +10v |
| Settling time, (10v step): | 50 μsec |
| Output current: | 10 ma |
| Capacitive loading: | 0.1 μf (without oscillation) |

| Binary Dig. In. | Analog Out | BCD (8421) | Analog Out |
|---|---|---|---|
| 000 — 00 | 0.0000v | 000 | 0.000v |
| 000 — 01 | +0.0025 | 001 | +0.010 |
| 100 — 00 | +5.0000 | 050 | +0.500 |
| 111 — 11 | +9.9975 | 500 | +5.000 |
| | | 999 | +9.990 |

| **Accuracy** | Binary | BCD |
|---|---|---|
| At +25°C: | ±0.015% of full scale | ±0.05% of full scale |
| Temp. coef: | ±0.001%/°C (plus drift of REF) | ±0.002%/°C (plus drift of REF) |

**Board Size**

1 double height board, single module width

**Temperature Range**

+10°C to +50°C

**Power**

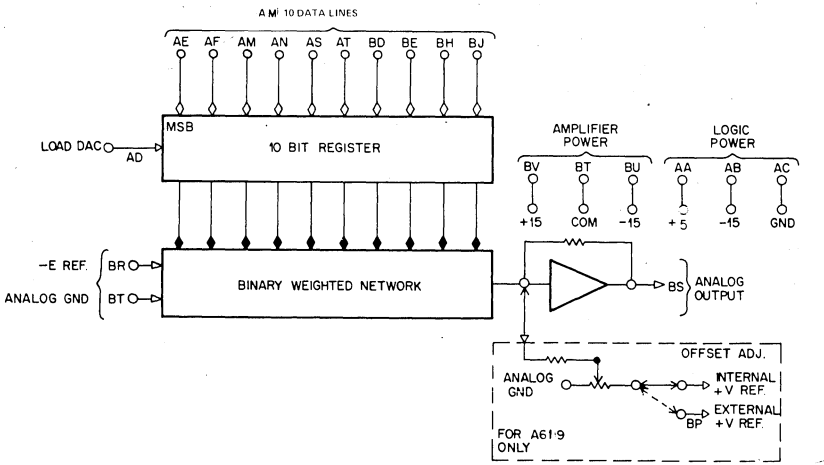
+15v at 35 ma
−15v at 60 ma } at max. load
+ 5v at 60 ma
−10.0v REF at −7 ma (reverse current)

If the Output is accidentally shorted to Ground, the output amplifier will not be damaged.

A613 — $250

# 10-BIT D/A CONVERTER SINGLE BUFFERED
## A618 and A619

**A SERIES**




The A618 and the A619 Digital to Analog Converters (DAC) are contained on one DEC double Flip-Chip™ Module. These modules are also double width in the lower (B section) half. The converters are complete with a 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier capable of driving external loads up to 10 ma. The reference voltage is externally supplied for greatest efficiency and optimum scale factor matching in multi-channel applications.

The A619 DAC output voltage is bi-polar while the A618 DAC output voltage is uni-polar.

Binary numbers are represented as shown (right justified) in Table 1:

**TABLE 1**

| Binary Input | Analog Output (Standard) | |
|---|---|---|
| | A618 | A619 |
| $0000_8$ | 0v | −10v or −5v |
| $0400_8$ | +2.5v | −5v or −2.5v |
| $1000_8$ | +5.0v | 0 volts |
| $1400_8$ | +7.5v | +5v or +2.5v |
| $1777_8$ | +10.0v | +10v or +5v |

**OUTPUT:**

| | |
|---|---|
| Voltage: (A618 — Standard) | 0 to +10 volts |
| Voltage: (A619 — Standard) | ±5 or ±10 volts |
| Current: | 10 ma MAX. |
| Impedance: | <0.1 ohm |
| Settling Time: | |
| (Full scale step, resistive load) | <5.0 μsec |
| (Full scale step, 1000 pf) | <10.0 μsec |
| Resolution: | 1 part in 1024 |
| Linearity: | ±0.05% of full scale |
| Zero Offset: | ±5 mv MAX. |
| Temperature Coefficient: | <0.2 mv/°C |
| Temperature Range: | 0 to 50°C |

**INPUT**

Level: 1 TTL Unit Load
Pulse: (positive)

| | |
|---|---|
| Input loading: 20 TTL Unit load | |
| Rise and Fall Time: | 20 to 100 nsec |
| Width: | >50 nsec |
| Rate: | $10^6$ Hz max. |

Timing:

Data lines must be settled 40 nsec before the "LOAD DAC" pulse (transition) occurs.

**POWER REQUIREMENTS:**

| | |
|---|---|
| Reference Power: | −10.06 volts, 60 ma |
| Amplifier Power: | ±15 volts, 25 ma (plus output loading) |
| Logic Power: | +5 volts, 135 ma |
| | −15 volts, 60 ma |

NOTES:

*Voltage — A619: Full scale voltage (±5 or ±10) must be specified at time of purchase.

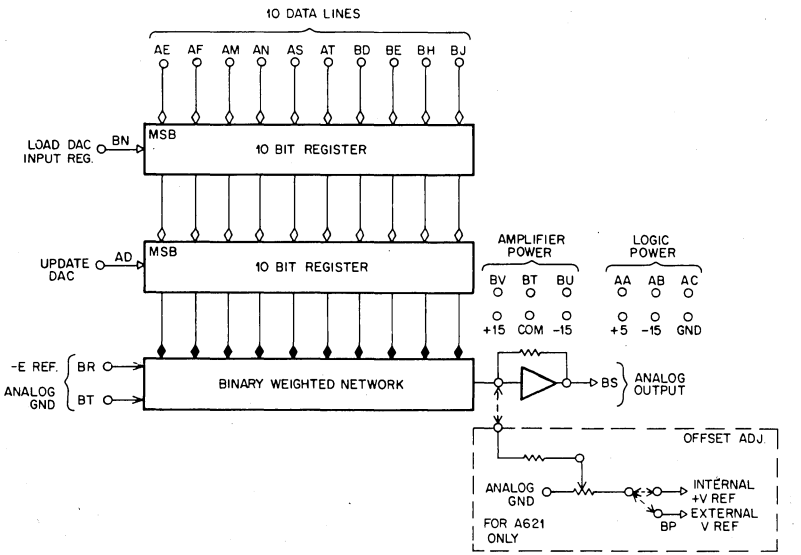
Price: Price stated is for standard output voltage and current. Other output characteristics are available on request.

A618 — $350
A619 — $375

# 10-BIT D/A CONVERTER DOUBLE BUFFERED

**A620 and A621**

**A SERIES**




The A620 and the A621 Digital-to-Analog Converters (DAC) are contained on one DEC double Flip-Chip Module. These modules are also double-width in the lower (B section) half. The converters are complete with two 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier, capable of driving external loads up to 10 ma. The reference voltage is externally supplied for greatest efficiency and optimum scale-factor matching in multi-channel-application.

The A621 DAC output voltage is bi-polar while the A620 DAC output voltage is uni-polar.

The double-buffered DAC's are offered to satisfy those applications where it is imperative to update several analog output simultaneously. When DAC's deliver input to a multi-channel analog tape system or update the constants of an analog computer, the double-buffer feature may be necessary to prevent skew in the analog data.

Binary numbers are represented as shown (right justified) in Table 1:

**TABLE 1**

| Binary Input | Analog Output (Standard) | |
|---|---|---|
| | A620 | A621 |
| $0000_8$ | 0v | −10v or −5v |
| $0500_8$ | +2.5v | −5v or −2.5v |
| $1000_8$ | +5.0v | −0 volts |
| $1500_8$ | +7.5v | +5v or +2.5v |
| $1777_8$ | +10.0v | +10v or +5v |

**OUTPUT:**

| | |
|---|---|
| Voltage: (A620 — Standard) | 0 to 10 volts |
| Voltage: (A621 — Standard*) | ±5 or ±10 volts |
| Current: | 10 ma MAX. |
| Impedance: | <0.1 ohms |
| Settling Time: | |
| (Full scale step, resistive Load) | <5.0 μsec |
| (Full scale step, 1000 pf) | <10 μsec |
| Resolution: | 1 part in 1024 |
| Linearity: | ±0.05% of full scale |
| Zero Offset: | ±5 mv MAX. |
| Temperature Coefficient: | <0.2 mv/°C |
| Temperature Range: | 0 to 50°C |

**INPUT:**

Level: 1 TTL Unit load

| | |
|---|---|
| Pulse: (positive) | |
| Input loading: | 20 TTL Unit load |
| Rise and Fall Time: | 20 to 100 nsec |
| Width: | > 50 nsec |
| Rate: | $10^6$ Hz MAX. |

Timing:

1. Data lines must be settled 40 nsec before the "LOAD DAC" pulse (transition) occurs.
2. The "Update DAC" pulse must occur more than 100 nsec after the "LOAD DAC" pulse.

**POWER REQUIREMENTS:**

| | |
|---|---|
| Reference Power: | −10.06 volts, 60 ma |
| Amplifier Power: | ±15 volts, 25 ma (plus output loading) |
| Logic Power: | + 5 volts, 190 ma |
| | −15 volts, 60 ma |

**Notes:**

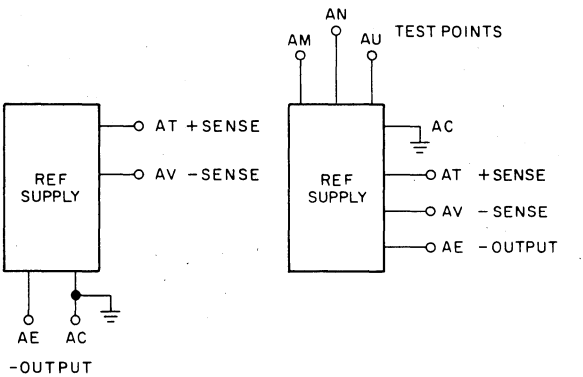
*Voltage — A621: Full scale voltage (±5 or ±10) must be specified at time of purchase.

Price: Price stated is for standard output voltage and current. Other output characteristics are available on request.

A620 — $400
A621 — $425

# REFERENCE SUPPLIES
## A702, A704
## (DOUBLE HEIGHT)

**A SERIES**




| Module Type | Output | Current | Temperature Coefficient | Regulation | Ripple Peak to Peak |
|---|---|---|---|---|---|
| A702 | −10 v | ±60 ma | 1mv/°C | 30 mv, no load to full load | 10 mv |
| A704 | −10 v | −90 to +40 ma | 1 mv/8 hrs<br>1 mv/15° to 35°C<br>4 mv/0° to 50°C | 0.1 mv, no load to full load | 0.1 mv |

| Module Type | Adjustment Resolution | Input Power | Use | Output Impedance |
|---|---|---|---|---|
| A702 | 5 mv | −15 v/100 ma<br>+10 v (B)/10 ma | Load with 500 μf at load. May also be preloaded if desired | 0.5 ohms |
| A704 | 0.01 mv | −15 ±2 v/250 ma | See below for sensing and preloading | 0.0025 ohms |

**Remote Sensing:** The input to the regulating circuits of the A704 is connected at sense terminals AT (+) and AV (−). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load. When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 μf should be connected across the load at the sensing point.

**Preloading:** The supplies may be preloaded to ground or —15v to change the amount of current available in either direction. For driving DEC Digital-Analog Converter modules, —125 ma maximum can be obtained by connecting a 270Ω±5% 1 watt resistor from the —10v pin AE reference output to pin AC ground (A704 only).

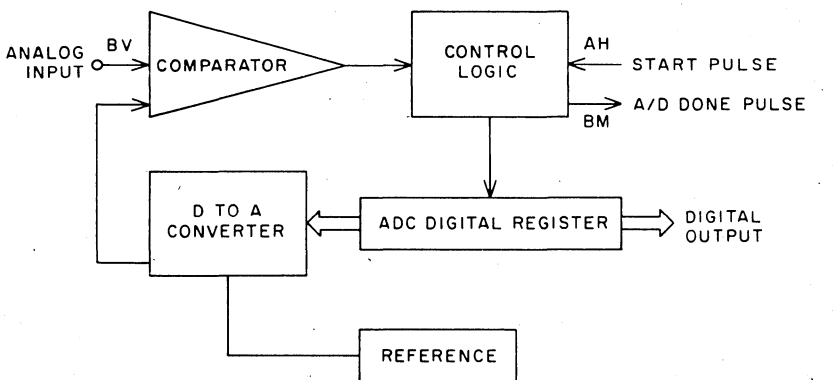
**Pin Connections:** The A704 is a double-sized module. The top pin letters are prefixed A.

**Wiring:** Digital-analog and analog-digital converters perform best when module locations and wiring are optimized. All Digital-Analog Converter modules should be side-by-side. In an analog-digital converter, the comparator should be mounted next to the converter module for the bits of most significance. The reference supply modules should be mounted nearby, and if the A704 is used, its sense terminals should be wired to the most-significant-bits converter module. The high quality ground must be connected to the common ground only at pin AC of the reference supply module, and this point should also be the common ground for analog inputs to analog-digital converters. Do not mount A-series modules closer than necessary to power suppply transformers or other sources of fluctuating electric or magnetic fields.

A702 — $ 58
A704 — $184

# 10 BIT A/D CONVERTER
A811

**A SERIES**



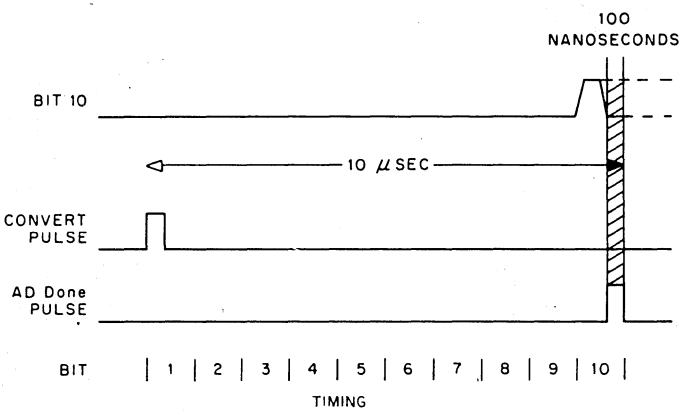

A811 10-BIT ANALOG-TO-DIGITAL CONVERTER

| | |
|---|---|
| BIT 1 (MSB) | AE |
| 2 | AD |
| 3 | AN |
| 4 | AM |
| 5 | BL |
| 6 | BR |
| 7 | BK |
| 8 | BP |
| 9 | BS |
| 10 (LSB) | BT |

## A811 10-BIT ANALOG-TO-DIGITAL CONVERTER

The A-811 is a complete, 10-bit successive approximation, analog to digital converter with a built in reference supply. The complete converter is contained on one DEC double FLIP CHIP™ logic module. Conversion is initiated by raising the Convert input to logic 1 (+4 volts). The digital result is available at the output within 10 microseconds. An A/D Done Pulse is generated when the result is valid. The A-811 uses monolithic integrated circuits for control logic, output register, and comparator.

The A811 requires 2 vertical connectors and the top section (connector A) requires 2 connector widths.




**SPECIFICATIONS:**

| | Max. | Min. |
|---|---|---|
| **Convert Pulse Input:** | | |
| Input loading | 10 TTL unit load | |
| Pulse Width | 500 nsec | 100 nsec |
| Pulse Rise Time | 250 nsec | — |
| **A/D Done Pulse Output:** | | |
| Pulse Width | 300 nsec | 100 nsec |
| **Digital Output:** | | |
| Logical "0" | +0.4v | 0v |
| Logical "1" | +3.6v | +2.4v |
| Output Current "0" | 16 ma | |
| Output Current "1" | −0.4 ma | |
| **Input:** | | |
| Input Voltage | 0 to +10v | |
| Input Impedance | 1000 ohms | |
| **Resolution:** | 10 bits | |
| **Accuracy:** | 0.1% of full scale | |
| **Temperature Coefficient:** | 0.5 mv/°C | |
| **Operating Temperature:** | 0°C to 50°C | |
| **Conversion Rate:** | 100 KHz MAX. | |
| **Output Format:** | Parallel Binary Uni-polar | |

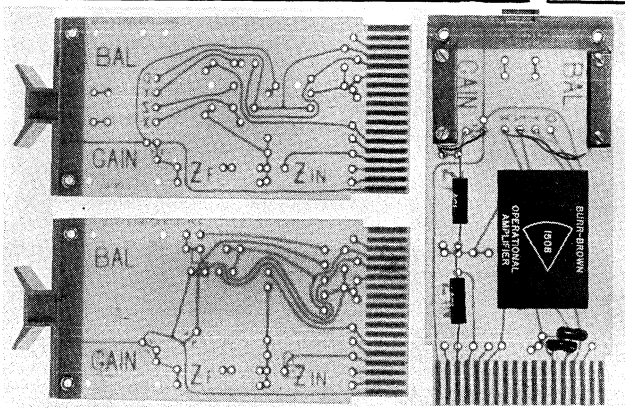
**Power:**
+15 volts ±1% 20 ma (pin BU)
−15 volts ±1% 160 ma (pin AV)
+ 5 volts ±1% 300 ma (pin AA)

**Options:**
The Input impedance of the A/D converter can be raised to greater than 100 megohms by adding an input amplifier module. A sample and hold amplifier module may also be included. The impedance of the converter with sample and hold is 10,000 ohms. Both options may be included simultaneously if high impedance and narrow aperture are both required.

A811 — $450

# AMPLIFIER BOARDS
## A990, A992

**A SERIES**



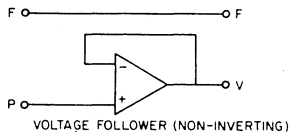

Many types of commercially available operational amplifiers can be mounted in the holes provided on these predrilled etched boards. Mounting holes and printed wires provide for balance trim, gain trim, and feedback networks required to build such common operational devices as voltage followers, inverting or non-inverting amplifiers, integrators, differentiators, summers and subtractors. Most amplifiers listed in the table below require ±15v regulated supplies which are readily available from the amplifier manufacturers. Notable exceptions are Analog Devices' Models 101, 103, and 104 which may be used with standard DEC +10v, −15v supplies at some sacrifice in voltage range (+5, −10v) and noise.

**Power:** Positive at pin D, negative at pin E, common at pin F for all types. Space is provided for mounting bypass capacitors used with some high frequency amplifiers.

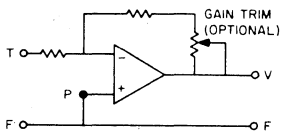
**Trimming:** Mounting holes on 1" centers at the handle end accept wirewound potentiometers for balance and feedback (gain) trimming. Gain rheostat may be connected in series with feedback components to allow precise adjustment of gain using inexpensive 1% feedback resistors. Board is etched to allow for use without gain trimming, and one pointed conductor must be cut at caret marks to put a rheostat in the circuit. Gain rheostat stray capacitance to ground is driven by amplifier output.

| Amplifier Supplier | Types accepted by A990 | Types accepted by A992 (boosters too) |
|---|---|---|
| Analog Devices | 101, 102, 104, etc. | 103, 106, 107, etc. |
| Burr-Brown* | 1500-46, 1500-68 | — |
| Data Device Corp. | — | most types, except boosters |
| Nexus | Case K or Case L | Case Q |
| Philbrick | — | Case PP |
| Union Carbide | — | most types |
| Zeltex | — | Case A |

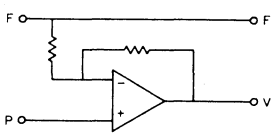
*Except Burr-Brown differential output and chopper stabilized types: Perforated board W994 or other blank module may be used to mount non-standard configurations.



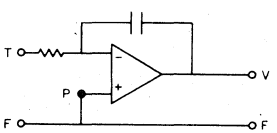
VOLTAGE FOLLOWER (NON-INVERTING)



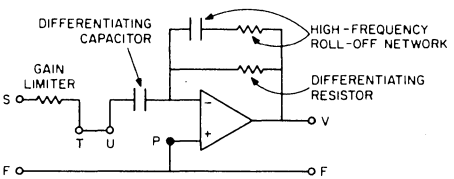
INVERTING AMPLIFIER



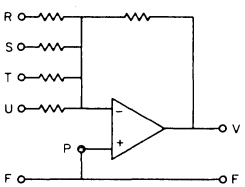
NON-INVERTING AMPLIFIER



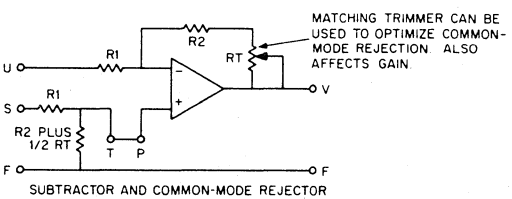
INTEGRATOR



DIFFERENTIATOR WITH DOUBLE BAND STOPS

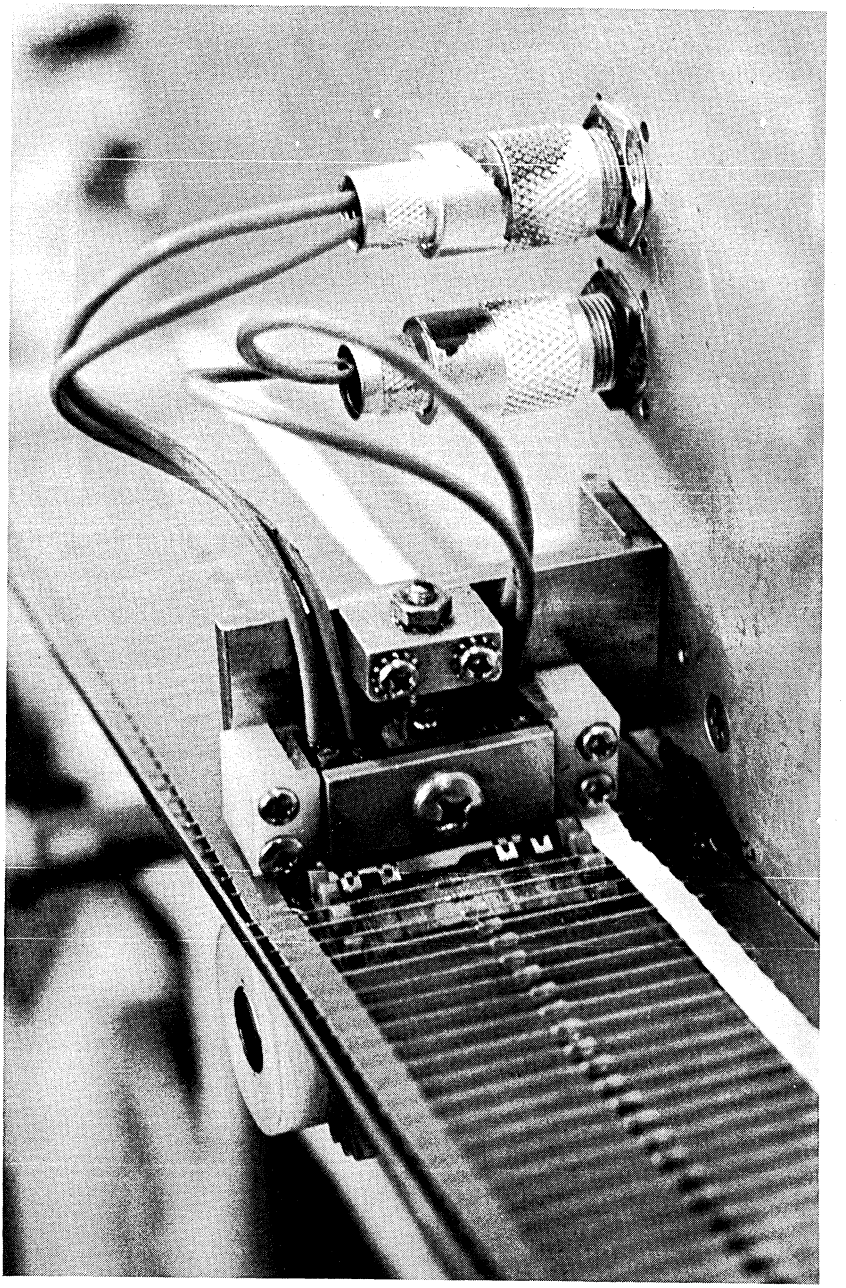


FOUR-INPUT SUMMER



SUBTRACTOR AND COMMON-MODE REJECTOR

A990 — $4
A992 — $4



All incoming components are 100% tested. Here, diodes are being tested automatically.

# B
# SERIES
# MODULE SUMMARY

## INVERTERS
**B104, B105, B123, B124**

**B SERIES**

Each inverter is analogous to a switch. If the inverter base is at −3 v and the inverter emitter is at ground, the transistor is saturated and a conducting path is established between the emitter and collector of the inverter. If the base is at ground, or if both base and emitter are at −3 v, the emitter-collector path is open circuited (i.e., will not allow current to flow).

Delay through the inverter is approximately 12 nsec for lightly loaded inverters driven by a pulse.

The B104 contains three standard 10-ma clamped loads and four transistor inverters, each with its base, emitter, and collector brought to connector pins.

The B105 has five standard 10-ma clamped loads and five transistor inverters, with each emitter grounded, and with each base and collector brought out.

The B123 has three standard 10-ma clamped loads and eight transistor inverters. The inverters are tied together in series groups of two.

The B124 has three standard 10-ma clamped loads and nine transistor inverters, each with emitter grounded, and with each base and collector brought to terminals. The collectors are tied together in groups of three.

B104 — $17
B105 — $21
B123 — $31
B124 — $31

## NAND/NOR GATES
**B113, B115, B117, B171**

**B SERIES**

The B113, B115, B117, and B171 are positive NOR diode gates; they form NOR gates for ground inputs and NAND gates for −3 v inputs. The outputs of the diode gates drive inverters similar to the B105, for power amplification. The typical total transition time is 40 nsec for output fall and 60 nsec for output rise. (Because the rise and fall delays differ, these diode gates may shorten negative input pulses markedly; see below.)

The B113 provides three standard 10-ma clamped loads and four diode gates, each with two diode inputs and the collector brought out.

The B115 has three standard 10-ma clamped loads and three diode gates, each with three diode inputs and the collector brought out.

The B117 has two diode gates, each with six diode inputs and the collector brought out. In addition, the emitter of one of the inverters is available.

The B171 is a single gate with twelve diode inputs. In addition to the positive NOR output, another inverter has been added at the output; using the inverted output makes the B171 an OR gate for ground inputs and an AND gate for −3 v inputs.

**Power:** B113: +10 v(A)/0.7 ma; −15 v(B)/43 ma; B115: +10 v(A)/0.5 ma; −15 v(B)/42 ma; B117: +10 v(A)/0.3 ma; −15 v(B)/2.5 ma; B171: +10 v(A)/0.3 ma; −15 v(B)/31 ma.

B113 — $23
B115 — $21
B117 — $14
B171 — $18

## THREE-BIT PARITY CIRCUIT
**B130**

**B SERIES**

This special logic module has two levels of high speed logic and complementary outputs. It is designed to compute the parity (odd or even) of the contents of a flip-flop register with a minimum of time delay, but it can be used wherever there is a need for four 3-input negative diode AND gates feeding a 4-input OR gate.

Delay is typically 15 nsec from 50% of the input transition to 50% of the output transitions when output capacitive loading is very small.

**Power:** +10 v(A)/49 ma; −15 v (B)/92 ma.

B130 — $50

## HALF BINARY-TO-OCTAL DECODER
**B155**

**B SERIES**

The B155 module is used alone as a 2-bit decoder with two enable inputs, or it is used with another B155 to form a full 3-bit (binary-to-octal) decoder, using one combined enable line. Either way, each binary input combination results in one selected output held at ground if the decoder is enabled. No output will be selected if an enable input is held at ground. The decoder consists of four 4-input diode gates with appropriate input interconnections. All of the output transistor emitters are connected to pin D, providing a third enabling point. Also included are four standard 10-ma clamped loads.

**Power:** +10(A)/0.6 ma; −15(B)/53 ma.

B155 — $21

## FLIP-FLOP
**B200**

**B SERIES**

Most 10 mc registers can be built with B200 buffered flip-flops. The delay from pulse input to flip-flop output is short, suiting the B200 for unidirectional counting and shifting applications in which comparators are used to stop the action. Delayed level inputs are conditional, providing JK characteristics. Some typical operations the B200 can perform at 10 mc input rates are: gated shifting, parallel-serial conversion, jam transfer, and simultaneous-transition counting. Typical delay: 30 nsec. Typical output rise time: 35 nsec. See "B Series — Logic Configurations" for examples of B200 applications.

**Power:** +10 v(A)/11 ma; −15 v(B)/45 ma.

B200 — $25

## FLIP-FLOP
**B201**

**B SERIES**

Some 10 mc operations require a greater variety of pulse inputs than the B200 can provide. For example, read-in from several sources, bi-directional shifting, and artihmetic operations all require the greater flexibility of the B201.

In order to allow the outputs to be sampled by the same pulse that is changing the state of the internal flip-flop, the buffers include a controlled amount of delay.

The B201 has nine built-in inverters for accomplishing such operations as set, clear, jam-transfer, shift, and complement without the need for additional gating. The B201 can also be used in counters. Logic diagrams for these operations are shown under "B Series Logic Configurations."

**Power:** +10(A)/5 ma; −15(B)/63 ma.

B201 — $56

## QUADRUPLE FLIP-FLOP
**B204**

**B SERIES**

Module B204 contains four bits of unbuffered flip-flop memory. Each flip-flop comprises two B105-type inverters, two 10-ma clamped loads, a common clear input, and an indicator driver resistor.

**Power:** +10(A)/0 ma; −15(B)/94 ma.

B204 — $29

## DELAY (ONE SHOT)
**B301**

**B SERIES**

A delay (one shot) is a monostable multivibrator. When the input terminal is grounded, either through the inverter or externally, the level output switches from its normal ground level to −3 v for a pre-determined, but adjustable, period of time; then it switches back to ground. Simultaneously with the final transition, a standard 40-nsec pulse is generated at the pulse output.

The B301 contains three capacitors for delay range selection, and a screwdriver-adjustable rheostat for fine control. Typical level output duration ranges are 60 to 700 nsec, 0.5 to 10 μsec, and 7 to 150 μsec using pins J, L, and V respectively. To increase the range further, connect an external capacitor between pins J and K. When pins U and P are jumpered together, fine adjustments are made with the internal control. For external control, a rheostat of about 5000 ohms can be connected between pins S and P.

The circuit recovery time using a given timing capacitor is approximately 10% of the maximum delay available with that capacitor. This limits the maximum input frequency to about 6.5 mc.

A 20% change in power supply voltage will change the delay typically 1%. Delay jitter (due to power supply ripple) is less than 0.3%.

**Power:** +10 v(A)/2 ma; −15 v(B)/110 ma.

B301 — $73

## DELAY
**B310 Double Height Board**

**B SERIES**

The B310 contains four delay lines, each producing maximum delay of 50 nsec in 12.5 nsec steps. The output of each line is connected to a transistor inverter whose emitter is grounded. The collector terminal is available for logical gating. The 15 nsec delay through the inverter must be added to the delay of the line.

**Power:** None required.

B310 — $66

## DELAY WITH PULSE AMPLIFIER
**B360**

**B SERIES**

The B360 contains a delay line which may be varied from 25 nsec to 250 nsec, and a standardizing pulse amplifier similar to one half of a B602. The length of the delay is adjusted by means of a slotted screw accessible from the handle-end of the module. The high resolution of the delay line (approximately ¼ nsec) makes it ideal for high-speed timing chains. By connecting the delay and pulse amplifier together with suitable logic in a feedback loop, a stable gateable clock may be obtained (see Application Section).

**Power:** +10 v(A)/5 ma; −15 v(B)/50 ma.

B360 — $84

## CLOCKS
**B401, B405**

**B SERIES**

The B401 Variable Clock produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies. The variable clock is often used as a primary source of timing for large systems. Where very precise timing is needed, the B405 Crystal Clock, which contains a single-frequency crystal oscillator, may be used.

The frequency of the B401 is variable from 10 kc to 10 mc. Three capacitors determine the frequency range, and a potentiometer provides fine control. For lower frequencies, an external capacitor may be used. When terminals U and P are connected together, the internal rheostat provides fine control. If desired, an external rheostat can be connected between terminals P and C. A 20% change in power supply voltage will change the frequency less than 1%. Pulse-to-pulse jitter is less than 0.3%.

The B405 contains a series resonant crystal oscillator circuit and a pulse-shaping buffer amplifier which produces standard 40-nsec pulses. The frequency, specified by the customer, can be between 2 and 10 mc. The frequency is stamped on the crystal. Stability is 0.01% over the temperature range of −20 to +55°C.

**Power:** B401: +10 v(A)/0 ma; −15 v(B)/70 ma. B405: +10 v(A)/51 ma; −15 v(B)/25 ma.

B401 — $ 57
B405 — $100

## PULSE AMPLIFIER
**B602**

**B SERIES**

The B602 contains two pulse amplifiers which are used for power amplification, for standardizing pulses in amplitude and width, and for transforming a level change to a pulse. Delay from the input of an inverter that drives the PA to the PA output is approximately 20 nsec. Input pulses may occur at any frequency up to 10 mc.

**Power:** +10 v(A)/2 ma; −15 v(B)/75 ma.

B602 — $36

## CARRY PULSE AMPLIFIER
**B620**

**B SERIES**

Module B620 supplements the B201 for 10-mc counting applications. It supplies the circuitry to complement two B201 Flip-Flops and propagate their carry pulses. One B620 and one B201 can also be combined to form one bit of an up-down counter. The B620 contains two pairs of inverters for complementing 10-mc flip-flops with conditional set and clear inputs, and two standardizing pulse amplifiers each capable of driving three inverter bases. The propagation delay is approximately 10 nsec. Maximum pulse repetition frequency is 5 mc for pulse amplifiers.

**Power:** +10 v(A)/6 ma; −15 v(B)/20 ma.

B620 — $47

## POWER INVERTER
**B681**

**B SERIES**

The B681 Power Inverter contains four high current inverters, each with separate emitter connections. A 20-ma clamped load is permanently connected to each collector. Four additional 10-ma clamped loads are supplied. Input and output current ratings are double those of a standard inverter.

**Power:** +10 v(A)/0 ma; −15 v/130 ma.

B681 — $25

## BUS DRIVER
**B684**

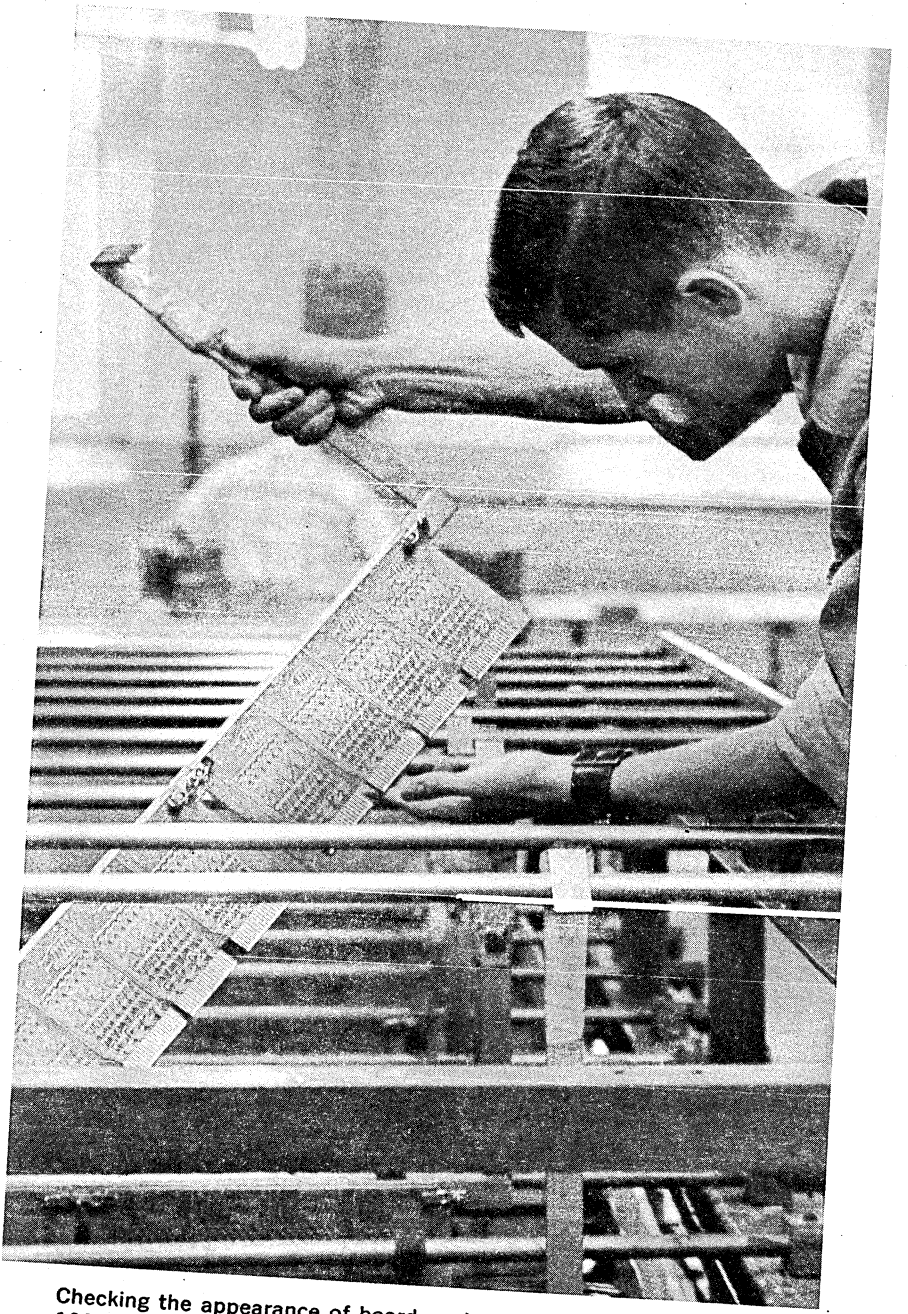
**B SERIES**

The B684 contains two dual-purpose, non-inverting bus drivers and a −3 v supply. Each bus driver provides standard levels either to a large number of inverter base and diode loads, or to a terminated 90-ohm cable. All logic terminals are available at the connector. Delay through a bus driver is approximately 30 nsec.

**Power Unloaded:** +10 v(A)/80 ma; −15 v(B)/120 ma.

**Power for Load:** Current to bring loads to ground must be added to the total demanded from +10(A); current to bring loads negative must be added to the total current from −15(B).

B684 — $52



Checking the appearance of board contacts being gold-plated. Our 100 micro-inch plating is verified by periodic checking on a radiation gauge.

# R
# SERIES
# MODULE SUMMARY

## DIODE NETWORKS
**R001, R002**

**R SERIES**

Diode networks can expand the logic capability of any R-Series, W-Series, or A-Series module which has one or more node inputs, such as the R111 diode gate. They can also make it possible to OR into an R-Series flip-flop output terminal for setting or clearing from several sources.

R001 — $4
R002 — $5

## INVERTER
**R107**

**R SERIES**

The R107 Inverter contains seven inverter circuits with single-input diode gates. Six of the circuits are used for single-input inversion; the seventh circuit can be used for gating by tying additional diode input networks to its node terminal. Clamped load resistors of 2 ma are a permanent part of each inverter.

**Power:** +10 v(A)/0.7 ma.; −15 v(B)/30 ma.

R107 — $24

## EXPANDABLE NAND/NOR GATE
**R111**

**R SERIES**

The R111 contains three diode gates, each connected to a transistor inverter. The gate operates as a NAND for negative inputs, and as a NOR for ground inputs. Each gate has three input terminals: two are connected to diodes, a third is connected directly to the node point of the diode gate. The third terminal allows the number of input diodes to be increased by adding external diode networks such as the R001 or R002. External diodes must be connected in the same direction as the diodes in the R111. Unused inputs may be left open.

**Power:** +10 v(A)/0.3 ma; −15 v(B)/18 ma.

R111 — $14

## NAND/NOR GATES
**R113, R121**

**R SERIES**

The R113 contains five diode gates, each connected to a transistor inverter. The gate operates as a NAND for negative inputs, and as a NOR for ground levels.

The R121 contains four R111-type circuits with 2-ma loads internally connected to each output. This module increases density at the expense of flexibility, since gate expanders R001 and R002 cannot be used.

**Power:** R113: +10 v(A)/0.5 ma; −15 v(B)/23 ma. R121: +10 v(A)/0.4 ma; −15 v(B)/20 ma.

R113 — $20
R121 — $17

## NOR/NAND GATE
**R122**

**R SERIES**

Provides the logical complement to the R121 NAND Gate at some sacrifice of speed and economy.

**Power:** +10 v(A)/3 ma; −15 v(B)/31 ma.

R122 — $26

## INPUT BUS GATE
**R123**

**R SERIES**

This module contains six R111-type diode gates arrayed for convenient driving of the PDP-8 computer input bus, and for other matrix-like applications. Clamped loads are not provided on this module, and must be obtained from some module in the associated logic.

**Power:** +10 v(A)/.6 ma; −15 v(B)/15 ma.

R123 — $19

## EXCLUSIVE OR
**R131**

**R SERIES**

This module provides a convenient way to compare two binary numbers or patterns. The output of each circuit is negative if its inputs are the same, and ground if they are different. If the outputs of several circuits are tied together, the common output line will be negative if every input pair matches, ground if any pair doesn't match.

**Power:** +10 v(A)/0.8 ma; −15 v(B)/36 ma.

R131 — $35

## AND NOR GATE
**R141**

**R SERIES**

The R141 AND/NOR Gate performs two levels of gating. The module contains a multiple-input diode gate with a transistor inverter for signal amplification. For negative input signals the R141 is seven 2-input AND gates which are NORed together. For ground inputs, it is seven 2-input OR gates NANDed together. This module is frequently used to mix multiple inputs to a pulse amplifier, or to compare the contents of two flip-flop registers.

**Power:** +10 v(A)/0.5 ma; −15 v(B)/19 ma.

R141 — $13

## BINARY-TO-OCTAL-DECODER
**R151**

**R SERIES**

The R151 decodes binary information from three flip-flops into octal form. When the enable input is at ground, the selected output line is at ground and the other seven outputs are at −3 v. When the enable input is at −3 v, all outputs are at −3 v. The internal gates are similar to those in the R111. The enable input is the common emitter connection of the output inverters. Typical total transition times are 75 nsec for output rise and 60 nsec for output fall.

**Power:** +10 v(A)/0.9 ma; −15 v(B)/32 ma.

R151 — $33

## DC CARRY CHAIN
**R181**

**R SERIES**

The R181 DC Carry module is designed for building counters with no carry propagation delay. A 2-mc counter of any size, with all flip-flops switching simultaneously, can be constructed using dc carry modules.

**Power:** +10 v(A)/0.7 ma; −15 v(B) /26.2 ma.

R181 — $35

## FLIP-FLOP
**R200**

**R SERIES**

The R200 is a basic flip-flop for use in set-reset applications. It can be set and cleared at any frequency up to 2 mc. A set input makes the 1 output go to −3 v and the 0 output to ground; a clear input makes the 0 output go to −3 v and the 1 output to ground.

**Power:** +10 v(A)/0.3 ma; −15 v(B)/16 ma.

R200 — $9.50

## FLIP-FLOP
**R201**

**R SERIES**

The R201 Flip-Flop has direct set and clear inputs and five diode-capacitor-diode (DCD) gates. Because of this large number of inputs, the R201 can be used in any of the following applications without additional gating.

1. Any two of the following as well as conditional read-in from an external source: up counter, shift register, jam transfer buffer, ring counter, and switch tail ring counter. Down counters or up-down counters can also be implemented if conditional read-in is not required.
2. BCD counter with read-in from two sources.
3. Buffer register or control flip-flop with read-in from five sources.
4. Special Counts of $2^R$ ($2^P + 1$).

**Power:** +10 v(A)/0.2 ma; −15 v(B)/27 ma.

R201 — $22

## DUAL FLIP-FLOP
**R202**

**R SERIES**

The R202 Dual Flip-Flop contains two identical flip-flops. Each has a direct clear input, a common set input, and two DCD gates. The R202 can perform in any one of the following applications without additional gating: up counter, down counter, shift register, ring counter, jam transfer buffer, and switch tail ring counter.

**Power:** +10 v(A)/0.5 ma; −15 v(B)/34 ma.

R202 — $25

## TRIPLE FLIP-FLOP
**R203**

**R SERIES**

The R203 Triple Flip-Flop contains three identical flip-flops. Each flip-flop has a direct clear input and a DCD gate for conditional read-in.

**Power:** +10 v(A)/0.7 ma; −15 v(B)/40 ma.

R203 — $28

## QUADRUPLE FLIP-FLOP
**R204**

**R SERIES**

The R204 Quadruple Flip-Flop contains four flip-flops. Each has direct set and direct clear inputs. Two of the flip-flops share a common direct clear input. The R204 is used in general control applications. A set input makes the 1 output −3v and the 0 output ground; a clear input makes the 0 output −3v and the 1 output ground.

**Power:** +10 v(A)/0.9 ma; −15 v(B)/42 ma.

R204 — $28

## DUAL FLIP-FLOP
**R205**

**R SERIES**

The R205 contains two identical flip-flops with a common direct clear input. Each has three DCD gates, and can be collector-triggered at either output by a diode-transistor gate or a diode network. The R205 can be used in any of the following applications without additional gating: up counter, down counter, shift register, ring counter, or jam transfer register.

**Power:** +10 v(A)/0.5 ma; −15 v(B)/36 ma.

R205 — $29

## DELAY (ONE SHOT)
R302

R SERIES

The R302 contains two delays (one-shot multivibrators) which are triggered by DCD gates. Each delay is independent and can be externally or internally controlled. When the input is triggered, the output changes from its normal ground level to −3v for a predetermined, adjustable period of time and then returns to ground. The length of the delay is determined by the capacitor and potentiometer. External capacitors can be attached between terminals H and J (or R and S), J (S) being the more positive terminal. The 20-kilohm internal potentiometer can be used by putting a jumper between terminals J and K (or S and T). External potentiometers can be attached between terminals J and L (S and U). The total resistance between these terminals must not exceed 20 kilohm. A 20% change in power supply voltage will change the delay less than 2%. Delay jitter due to power supply ripple is less than 0.2%.

**Power:** +10v(A)/0.6 ma; −15 v(B)/88 ma.

R302 — $44

## INTEGRATING ONE SHOT
R303

R SERIES

The R303 contains a zero recovery time multivibrator and complementary output buffers. Its unusual characteristics include the ability to respond to inputs even while in the ONE state, so that successive inputs above a preset frequency can postpone the return to ZERO indefinitely. This characteristic can be used, for example, to detect gaps in an otherwise continuous pulse. train, or to determine whether an input pulse rate is above or below a preset frequency threshold. If the delay setting of this module exceeds the time it takes +10 and −15 to reach 90% of their final valves on power turn-on, this module will initially go to the ONE state. The above conditions allow the R303 to be used for system initialization on power turn-on.

Delay is 3.5 microseconds to 0.7 second. Jitter is less than 1.4% peak-to-peak. Precision: Delay time will change less than 2% for a change of 20% in supply voltage.

**Power:** + 10v(A)/6 ma; −15 v(B)/75 ma.

R303 — $45

## VARIABLE CLOCK
**R401**

**R SERIES**

The R401 Variable Clock is a gateback clock that produces standard 100-or 400-nsec pulses from a stable RC-coupled oscillator. The variable clock is often used as a primary source of timing for large systems.

The frequency of the R401 Clock is variable from 30 cps to 2.0 mc. Five capacitors provide coarse frequency control, and a built-in 20,000 ohm potentiometer permits fine adjustment. Terminals for an external potentiometer or capacitor are available. The maximum size of the external potentiometer to be used is 20,000 ohms.

Lower frequencies may be obtained by adding an external capacitor between pins R and C. A 20% change in power supply voltage will change the prf less than 1%. The pulse-to-pulse jitter is less than 0.2%.

**Power:** + 10v(A)/6 ma; −15 v(B)19 ma.

R401 — $45

## CRYSTAL CLOCK
**R405**

**R SERIES**

The Type R405 employs a series resonant crystal oscillator, squaring circuit, and output pulse amplifier. The crystal clock's output frequency remains within 0.01% of specified value between 0°C and +55°C. The clock frequency is specified anywhere in the 5 kc to 2 mc range by the customer and is stamped on the crystal can.

**Power:** + 10v(A)/5.4 ma; −15 v(B)/50 ma.

R405 — $100

## PULSE AMPLIFIER
**R601**

**R SERIES**

The R601 is a pulse amplifier that standardizes pulses in amplitude and width. Outputs may be either standard 100- or 400-nsec pulses (−3v to ground). It has six DCD gates so that inputs from as many as six sources may

be mixed. Input pulses can occur at any frequency up to 2 mc for 100-nsec pulse outputs and up to 1 mc for 400-nsec outputs. Delay through the pulse amplifier is approximately 50 nsec.

**Power:** +10v(A)/1.1 ma; −15 v(B)/33 ma.

R601 — $25

## PULSE AMPLIFIERS
**R602, R603**

**R SERIES**

The R602 and R603 contain pulse amplifiers for power amplification and for standardizing pulses in amplitude and width. Each amplifier produces standard 100-nsec pulses and one section of the R602 can also produce 400 nsec pulses. DCD gates and a single diode input permit inputs from many sources to be mixed. Input pulses can occur at any frequency up to 2 mc for 100 nsec pulses, and up to 1 mc for 400 nsec pulses. Delay through the pulse amplifier is approximately 50 nsec.

**Power:** R602: +10v(A)/2.2 ma; −15 v(B)/45 ma.
R603: +10 v(A)/3.3 ma; −15 v(B)/57 ma.

R602 — $22
R603 — $28

## BUS DRIVER
**R650**

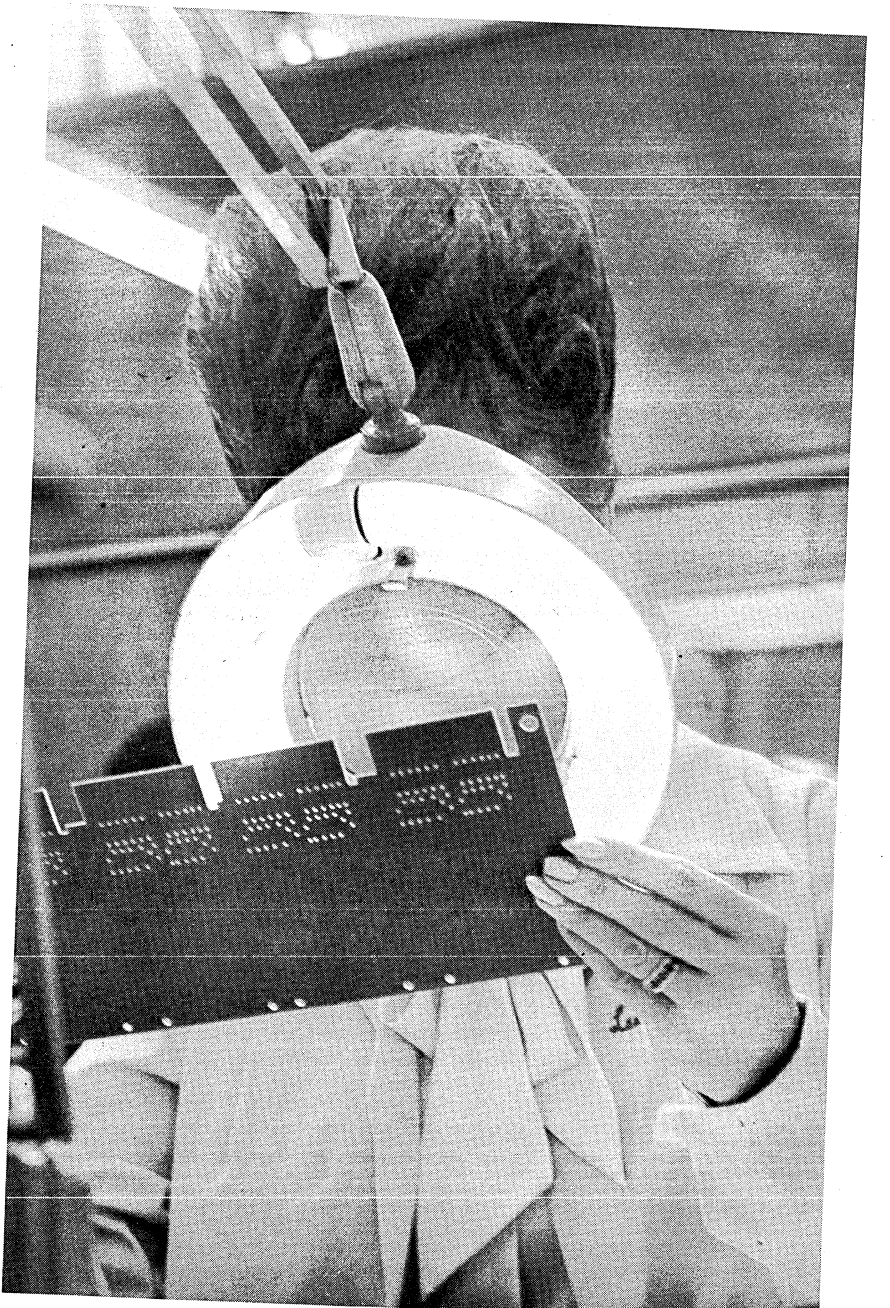
**R SERIES**

The R650 contains two inverting bus drivers for driving heavy current loads to either ground or negative voltages. The four input terminals make the R650 a versatile logic element as well. The diode inputs D and E (N and P) are the principal inputs. They form a NAND gate for negative inputs or a NOR gate for ground inputs. Gate inputs, such as the R001 or R002, can be added through the node terminal F (R). Other gating sources may be mixed with the gate inputs by using collector terminal L (V).

The bus drivers operate at frequencies up to 2 mc with typical rise and fall times of 25 nsec. The typical total transmission times are 60 nsec for output rise and 65 nsec for output fall.

**Power:** +10 v(A)/50 ma; −15v(B)/81 ma.

R650 — $23



Quality of plated-thru holes is checked in our new electrochemical facility before boards go to the module assembly area.

# W
# SERIES
# MODULE SUMMARY

## CLAMP LOADS
**W002, W005**

**W SERIES**

The W002 conatins 15, 2-ma clamped loads. These can be used for clamping voltages at the output of inverter collectors in R-Series modules, or for converting B-Series modules to work with R-Series.

The W005 contains 15, 5-ma clamped loads. These can be used for clamping voltages at the output of inverter collectors in B-Series modules, or for converting R-Series modules to work with B-Series. Two of these clamped loads in parallel are equivalent to one B-Series clamped load.

**Power:** W002: −15v (B)/46 ma. W005: −15v (B)/91 ma.

| |
|---|
| W002 — $13 |
| W005 — $15 |

## CABLE CONNECTORS FOR INDICATOR AMPLIFIERS
**W018, W023**

**W SERIES**

The W018 and W023 provide 18 line ribbon cable connections to FLIP CHIP mounting panels. In the W018 connection to each pin is through a series low leakage silicon diode. The W023 provides unbroken signal lines from the cable to the connector pin.

When these cables are used with 4917 or 4918 indicators, the W018 must be located at the FLIP CHIP panel and the W023 inserted in the indicator socket connector. Cables may be ordered with connector modules on both ends or on one end only. Cable length may be specified in increments of 1 inch.

Care should be taken when using the W023 for other purposes, since the Power Pins (A, B) are unprotected.

| | |
|---|---|
| | W018 — $ 9 |
| | W023 — $ 4 |
| With Cable | W018 — $18 |
| | W023 — $13 |

## SOLENOID DRIVERS
**W040, W043**

**W SERIES**

These high current drivers can drive relays, solenoids, stepping motor windings, or other similar loads. The output levels are- 2 volts and a more negative voltage determined by an external power supply. One terminal of the load device should be connected to the external power source, the other to the driver output. There are two drivers per module and both modules use the same pin connections.

**Power:** W040; +10 v(A)/0 ma; −15 v(B)/24 ma. The external voltage supply must supply the output current of the two drivers (1.2 amp max.)

**Power:** W043; +10 v(A)/0.25 ma; −15v(B)/6 ma. The external voltage supply must supply the output current (2.0 amp max.)

W040-$36
W043-$35

## 10 AMP DRIVER
**W042**

**W SERIES**

This module has four germanium transistor drivers each capable of providing up to ten amperes of DC drive at ambients up to 40°C for heavy loads such as paper tape punches, card punches, hydraulic servo valves, or high-torque stepping motors like Responsyn (T.M. United Shoe) or Slo-Syn (T.M. Superior Electric). In 55°C ambients up to 8 amps total current may be obtained. AMP "Faston" tabs at the handle end of the module provide high current connections for ground, ES, and the four outputs and external ground. Due to the fact that this module may dissipate as much as 20 watts when operated at rated output, special consideration should be given to an unobstructed flow of cooling air.

**Power:** +10v (A)/180 ma; ES/270 ma plus output current

W042-$80

## 30 MA INDICATOR DRIVER
**W050**

**W SERIES**

The W050 contains seven transistor amplifiers that can drive miniature incandesecent bulbs, such as those on an indicator panel. It is used to provide remote indicators for R- or B- Series flip-flops. If the input is at −3v, the output is at −1v.

**Power:** +10v (A)/1.1 ma; −15v (B)/7 ma.

W050 — $13

## 100 MA INDICATOR AND RELAY DRIVER
**W051**

**W SERIES**

The W051 contains seven inverter amplifiers suitable for driving indicators, relays and other medium power devices. The amplifiers can supply up to 100 ma at ground, and each output is diode clamped to 15v to prevent overvoltage when the current is interrupted in an inductive load. If the input is at −3v, the output is at ground. Typical delay for circuit alone: 1 microsecond.

**Power:** +10v (A)/3 ma; −15v (B)/23 ma.

W051 — $22

## RELAY DRIVER
**W061**

**W SERIES**

The W061 Relay Driver has four all-silicon 250 ma drivers with gateable inputs; it can drive relays and solenoids with positive voltage supplies up to 55v. Typical delay for circuit alone: 1 microsecond.

**Power:** +10v (A)/70 ma; −15v (B)/8 ma.

W061 — $35

## ISOLATED AC-DC SWITCH
**W080**

**W SERIES**

This module contains two photon-coupled transistor switches with bridge rectifiers. Both turnon and turnoff are slow enough to minimize output noise. Output tabs are at handle end of module for maximum isolation. Drives relays, solenoids, panel lamps, small motors directly. Larger AC loads can be driven by the use of SCR or Triac* buffers. For example, one SC45B Triac with a W080 circuit tied from gate to anode 2 and a 100Ω resistor from gate to anode 1 can switch AC loads up to one kilowatt. Switching rate must not exceed 1 hertz. Switching time: 1/10 second.

**Power:** 10v (A)/60 ma; −15v (B)/0.

*G. E. Trademark

W080-$60

## PDP-8 DEVICE SELECTOR
**W103**

**W SERIES**

This module is used to decode the six device selector bits transmitted in complement pairs on the PDP-8 or PDP-8/S I/O bus, and it provides standard pulses to the selected device. The device code is selected by cutting one diode of each pair, BE or BF, etc. off the board. Device coding can also be accomplished by selective wiring of the bus inputs to the diode pairs.

**Power:** +10v (A)/6.4 ma; −15v (B)/57 ma.

W103 — $52

## DECODING DRIVER
**W108 (DOUBLE HEIGHT)**

**W SERIES**

This driver provides up to 300 ma bipolar drive currents for use in memory systems including core memories, such as the H201 and magnetic tape systems. There are eight drivers on a module, each of which can be selected

either by one of eight address lines or by using the built-in binary-to-octal decoding matrix. The drive current direction is selected by one of two input select lines and will be the same for all drivers on a module. Drive current can be varied from 160 ma to 300 ma by adjusting the external negative voltage reference connected to a tab terminal on the module handle.

**Power:** −15 (B)/16 ma plus 35 ma per selected driver
−V(TAB)/maximum of 250 ma per negative current driver used.

W108 — $75

## HIGH IMPEDANCE FOLLOWER
**W500**

**W SERIES**

High impedance signal sources such as photocells and low current instrumentation amplifiers can drive Schmitt Trigger W501 or logic gates through a W500 circuit. The module contains 7 fault-protected circuits, each comprising two cascaded emitter-follower amplifiers. Input voltage excursions up to ±30v or short-circuits from output to ground are harmless. Outputs can go as negative as −15v with very light loading, but will not exceed −10v when driving a W501 input.

**Power:** +10v (A)/18 ma; −15v (B)/35 ma.

W500 — $25

## NEGATIVE INPUT CONVERTER AND SCHMITT TRIGGER
**W501**

**W SERIES**

The W501 contains a Schmitt trigger circuit which produces standard levels as a result of some outside activity such as the closure of a switch or relay. A ground level input produces a −3v level output, and a negative level input produces a ground level output. Norminal switching thresholds of −2.2v and −0.8v are obtained by connecting terminal L to terminal K and terminal M to terminal N. The switching thresholds can be varied over the range of 0 to −2.5v by applying external voltage levels to terminals M and L. Terminal M controls the lower level threshold, and terminal L controls the upper level threshold. The module also contains an integrating circuit to filter contact bounce when a switch or relay is used to generate the levels.

**Power:** +10v (A)/12 ma; −15v (B)/27 ma.

W501 — $13

## POSITIVE INPUT CONVERTER
**W510**

**W SERIES**

The type W510 Positive Level Converter contains three circuits that convert positive levels to DEC standard levels of ground and −3v. Each circuit consists of a grounded-emitter inverter with a diode string between its input and the base of the inverter. By shorting out sections of the diode string, the switching threshold may be varied to either +2v, +1v, or 0. When the input is more positive than the switching threshold by 1v, the inverter is cut off and the output is at −3v. When the input is more negative than the switching threshold by 1v, the inverter is saturated and the output is at ground.

**Power:** +10v (A)/8.0 ma; −15v (B)/17 ma.

W510 — $17

## NEGATIVE INPUT CONVERTER
**W511**

**W SERIES**

The type W511 Negative Level Converter contains two circuits that convert negative levels to DEC standard levels of ground and −3v. Each circuit consists of a grounded emitter inverter with a string of bias diodes between its base and the input pins. A separate input diode is also provided. By connecting the input diode to various points on the diode string, the switching threshold can be set at Ov, −1v, −2v, or −3v. When the input is more positive than the switching threshold by 1v, the inverter is cut off and the output is at −3v. When the input is more negative than the switching threshold by 1v, the inverter is saturated and the output is at ground.

**Power:** +10v (A)/3 ma; −15v (B)/24 ma.

W511 — $17

## POSITIVE LEVEL CONVERTER
**W512**

**W SERIES**

Positive logic systems, such as those being monolithic integrated circuits, can use the W512 to make available standard accessory modules in the W and A Series.

Input threshold voltage to each converter is normally 1.6 volts for compatibility with DTL and TTL levels. This threshold can be set at 0.8 volts by grounding pin V for RTL level conversion.

**Power:** +10v (A)/104 ma; −15v (B)/30 ma.

W512 — $25

## COMPARATOR
**W520**

**W SERIES**

This module is useful as an inexpensive comparator for A/D work, or as a general-purpose input level converter. The W520 contains three four-transistor difference amplifiers which give DEC standard levels at the output. The state of the output is determined by the relative polarity of the input voltages.

Max delay for output fall:
75ns. 50% to 50%
Max delay for output rise:
150ns. 50% to 50%
Typical rise time 10%
to 90%: 25ns
for 200mv square wave
about a fixed reference
voltage

The W520 is tested for 100mv difference minimum. It is not a replacement for the more precise A502.

**Power:** +10v (A)/37 ma; −15v (B)/32 ma.

W520 — $43

## DUAL AC-COUPLED DIFFERENCE AMPLIFIERS
**W532**

**W SERIES**

The W532 contains two AC-coupled differential amplifiers for use with many magnetic sense systems, including the H201 core memory. These amplifiers provide the high differential gain and common mode noise rejection necessary to amplify information signals in a system using a single sense line per plane for a memory or per channel for a tape system.

**Power:** +10v (A)/40 ma; −15v (B)/40 ma.

W532 — $30

## DUAL RECTIFYING SLICER
**W533**

**W SERIES**

This module is used to detect amplified magnetic system sense signals from a W532 and convert them to positive DEC pulses. Detection of signals as narrow as 100 nsec is possible over a wide range of detection thresholds. There are two slicer circuits on each W533. Two input terminals per circuit permit rectification so that bipolar difference signals can be sliced and standardized.

**Power:** +10v (A)/40 ma; −15v (B)/28 ma.

W533 — $30

## IBM N LINE TO DEC CONVERTER
**W590**

**W SERIES**

Each of the 5 inverting amplifiers on this module provides input characteristics compatible with three types of IBM N Lines. Input impedance is nominally 300 ohms, with 100 ohm impedance available by connecting 150 ohm shunts provided. Each circuit has a switching threshold near zero volts, with input biasing included to maintain a definte output state when the input is open-circuited.

Unshunted inputs will tolerate input excursions up to +4v and −6v, so these circuits may also be used to convert IBM T, D, or Q lines if the IBM circuits involved can safely drive the W590 input loads.

**Power:** +10 v (A)/40 ma; −15v (B)/23 ma.

W590 — $26

## NEGATIVE OUTPUT CONVERTER
**W600**

**W SERIES**

The W600 contains three inverting amplifiers that convert standard levels to outputs of ground and an externally supplied negative voltage. The external clamp voltage is applied to terminal F (M, T) and must be between −1 and −15v. Additional inputs may be added by tying diode networks, such as, those contained on the R001 or R002, to the node terminal. These inputs form a NOR gate for ground levels and a NAND gate for negative levels. That is, if any input diode is at ground, the output is at the external clamp voltage: and if all inputs are at −3v, the output is at ground. Output rise and fall TTT are less than respectively 100 and 200 nsec.

**Power:** +10v (A)/0.3 ma; −15v (B)/33 ma.

W600 — $12

## POSITIVE OUTPUT CONVERTER
**W601**

**W SERIES**

The W601 contains three amplifiers for converting DEC standard levels to outputs of ground and an externally supplied clamp voltage level, $E_c$. This external clamp voltage is applied to terminal F (M) and must be between +1 and +20v. Additional inputs can be added by tying diode networks, such as, the R001 or the R002, to the node terminal. These inputs form a NOR gate for ground levels and a NAND gate for negative input levels. That is, if any input diode is at ground, the output will be at ground and if all inputs are −3v, the output will be at $E_c$. A positive supply voltage $E_s$ greater than $E_c$ should be tied to terminal V. If $E_c$ is less than +10v, the +10v supply on terminal A may be used at the supply voltage on terminal V. Output rise and fall TTT are less than respectively 150 and 100 nsec.

**Power:** +10 v(A)/3 ma; −15 v(B)/6 ma.

W601 — $13

## BIPOLAR OUTPUT CONVERTER
**W602**

**W SERIES**

For driving EIA standard communication lines and other applications demanding levels both positive and negative with respect to ground the W602 provides up to 15 ma at up to 6 v. There are three inverting amplifiers on the module. To control noise on long transmission lines the output rise and fall times are intentionally slowed to roughly 50 nsec/v, and at low repetition rates capacitance may be connected externally from outputs to ground to further increase rise and fall times. Output upper levels can be set at 6 v, 3 v, or 0 v, and lower levels can be set at 6 v, 3 v, or 0 v using clamp voltage supplies provided.

**Power:** +10 v(A)/32 ma; −15 v(B)/31 ma.

W602 — $40

## POSITIVE LEVEL AMPLIFIER
**W603**

**W SERIES**

Positive logic systems such as those using RTL, DTL, or TTL monolithic integrated circuits can be driven from FLIP CHIP systems through the W603. Clamped load resistors at the output of each circuit permit output levels to be adjusted to the type of circuit being driven. Normally the clamp voltage at pin V is provided by the logic supply voltage used with the monolithic circuits. This clamp voltage is common to all seven converters on the module.

**Power:** +10 v(A)/35 ma.; −15 v(B)/7 ma.

W603 — $23

## PULSE OUTPUT CONVERTERS
**W607 AND W640**

**W SERIES**

These pulse converters were designed primarily to facilitate the use of FLIP CHIP modules in conjunction with Digital Laboratory and System Modules. In addition, the W607 can be useful in setting or clearing B Series unbuffered flip-flops via inverters such as B104 or gates such as B113.

Outputs from these pulse converters are taken from floating pulse-transformer windings. In addition to allowing data transmission independent of ground system integrity, this feature permits two or three outputs to be series-connected for larger pulse amplitudes when inputs are driven simultaneously.

**Power:** W607: +10 v(A)/0 ma.; −15 v(B)/35 ma. W640: +10 v(A)/0 ma.; −15 v(B)/25 ma.

W607 — $42
W640 — $42

## DEC TO IBM N LINE CONVERTER
**W690**

**W SERIES**

Each of the four inverting drivers on this module provides outputs compatible with the three types of IBM N lines, depending upon what output currents are programmed by grounds or open circuits at pins T and U. Node points are provided at each input. Maximum delay: 100 nanoseconds driving N transmission lines.

Outputs will drive loads returned to voltages as high as +12 volts so this module will also drive T, D, or Q lines with suitable biasing networks added.

**Power:** +10v (A)/0 ma; −15v (B)/150 ma.

W690 — $36

## SWITCH FILTER
**W700**

**W SERIES**

The W700 contains six switch filters for reducing contact closures to standard levels. The output drive of the switch filter is determined by the voltage to which the switch contact is returned.

**Power:** Terminal D connected to −15v: +10v (A)/0 ma; −15v (B)/31 ma.
Terminal D connected to +10v: +10v (A)/8 ma; −15v (B)/22 ma.

W700 — $20

## POWER SUPPLY (+3.6 volt)
**W705 (SINGLE HEIGHT, TRIPLE WIDTH)**

**W SERIES**

This inexpensive power supply is of primary use in conjunction with the W706 and W707 teletype modules. The output can supply up to 1.5 amps at a

nominal voltage of 3.6 volts. Voltage regulation for variable loading is provided and output ripple is less than 40 mv.

**Power:** +10v (A)/200 ma, plus load current

W705 — $15

## TELETYPE RECEIVER
### W706 (DOUBLE HEIGHT)

**W SERIES**

The W706 Teletype Receiver is an integrated-circuit, series-to-parallel Teletype code converter, self contained on a double-height module. This unit includes all of the serial to parallel conversion, buffering, gating and synchronizing necessary to transfer information between an incoming asynchronous serial teletype line and a parallel binary device. Either a 5 bit serial character consisting of 7.0, 7.5 or 8.0 units or an 8 bit serial character of 10.0, 10.5 or 11.0 units can be assembled into parallel from by the W706 through the use of selective jumpers on the module.

**Power:** −15 (B) 12 ma: +3.6 v 550 ma. This power is available from a W705 or any commercial supply that has an output regulation of ±10%.

W706 — $150

## TELETYPE TRANSMITTER
### W707 (DOUBLE HEIGHT)

**W SERIES**

The W707 Teletype Transmitter is an integrated circuit parallel to serial teletype code converter, self contained on a double-height module. This unit includes all of the parallel to serial conversion, buffering, gating, and timing necessary to transfer information in an asyncronous manner between a parallel binary device and a serial teletype line. Either a 5 bit or 8 bit parallel character can be assembled into a 7.0, 7.5 or 8.0 unit serial character or a 10.0, 10.5 or 11.0 unit serial character, respectively, by the W707 through the use of selective jumpers on the module.

**Power:** −15 (B)/3 ma: +3.6 v/550 ma. This power is available from a W705 or any commercial supply that has an output regulation of ±10%.

W707 — $150

## TELETYPE INTERFACE
**W708**

**W SERIES**

The W708 provides special gating controls and clock synchronization for teletype and data communications systems when used with the W706 and W707 teletype modules. Such system features as half duplex operation, half unit start bit spike rejection and single clock operation are possible when W706, W707 and W708 modules are used in a system. DIGITAL's Application Note AP-W-001 shows several system interconnections using a W708.

**Power:** −15v (B)/25 ma; +3.6 v/300 ma. This power is available from a W705 or any commercial supply that has an output regulation of ±10%.

W708 — $55

## DIVIDE BY 16/64 COUNTER
**W709**

**W SERIES**

The W709 module provides the count-down circuitry for conversion of stable crystal clock frequencies to low frequencies common to teletype and data communications systems.

**Power:** −15 (B)/27 ma; +3.6 (J)/180 ma. This power is available from a W705 or any commercial supply that has an output regulation of ±10%.

W709 — $30

## RELAY
**W800**

**W SERIES**

The W800 Relay consists of two separate Form A reed relays, each with an optional protecting circuit. When the protecting circuit feature is desired, N and P (T, U) should be connected together and the external circuit connected to P and R (U, V). To use the relay without the protecting circuit, the external circuit should be connected between M and R (S, V). The protecting circuit consists of a capacitor and a parallel combination of an inductor and a

resistor. The protection circuit slows down current and voltage rise time at the time of contact closure or opening in order to minimize undesirable effects on sensitive logic in the vicinity of the relay. The type W800 is used to drive heavy loads on computer or logic command. The frequency limit is 100 cps. Maximum relay operating time is 2 msec.

**Power:** 15v/124 ma; +10v (A)/0.6 ma.

W800 — $45

## RELAY MULTIPLEXER
### W802 (DOUBLE HEIGHT MODULE)

**W SERIES**

The W802 Relay Multiplexer contains eight double-pole, normally open reed relays. One of its uses is to address memory lines in memory testers. It can also be used as a low-speed multiplex switch where the grounded, low-noise performance of the A111 multiplexer is not required. Maximum closing time: 1.5 msec; typical opening time 500 μsec.

**Power:** +10v (A)/2 ma; −15v (B)/20 ma plus 25 ma per energized relay (220 ma max. for all relays energized).

W802 — $160

## BLANK MODULES
### W970-W975, W990-W995

**W SERIES**

These 12 blank modules offer convenient means of integrating special circuits and even small mechanical components into a FLIP CHIP system, without loss of modularity. Both single and double size boards are supplied with contact area etched and gold plated. The W990 Series modules provide connector pins on only one module side for use with H800 connector blocks. W970 Series modules have etched contacts on both sides of the module for use with double density connectors type H803.

| | |
|---|---|
| W990 | $ 2.50 |
| W991 | $ 5.00 |
| W992 | $ 2.00 |
| W993 | $ 4.00 |
| W994 | $ 4.50 |
| W995 | $ 9.00 |
| W970 | $ 4.00 |
| W971 | $ 8.00 |
| W972 | $ 4.00 |
| W973 | $ 6.00 |
| W974 | $ 9.00 |
| W975 | $18.00 |

## MODULE EXTENDER
**W980**

**W SERIES**

The W980 Module Extender allows access to the module circuit without breaking connections between the module and mounting panel wiring.

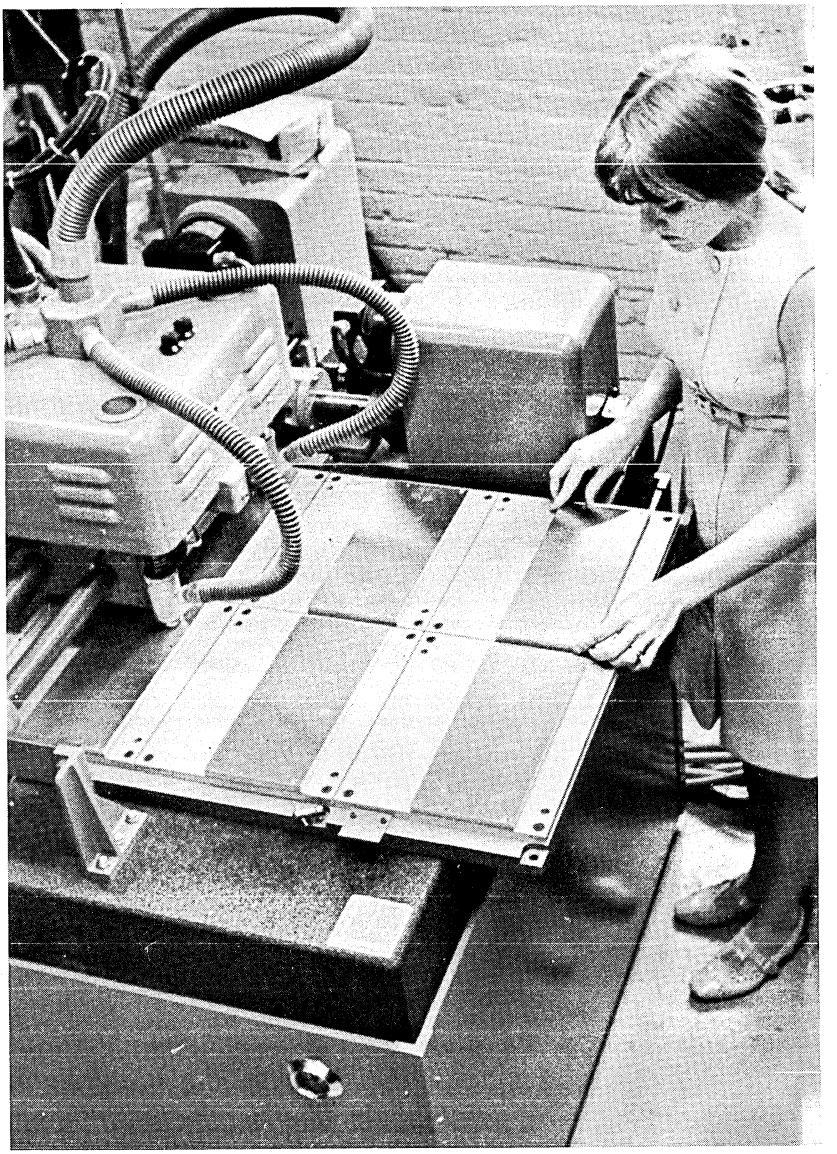
W980 — $14

## SYSTEM MODULE ADAPTER
**W985**

**W SERIES**

The W985 is an adapter which permits DEC system modules to be plugged into a FLIP CHIP mounting panel. It requires a block of four (two high and two wide) FLIP CHIP module spaces.

W985 — $34



Twenty module boards are drilled simultaneously from a computer-generated coordinate tape. Other pantograph-controlled machines drill up to 200 boards simultaneously from a computer-generated template.

# PART II
# UNIVERSAL HARDWARE, POWER SUPPLIES AND ACCESSORIES

# INTRODUCTION

Digital manufactures a complete line of hardware accessories in support of its module series. Module connectors are available for as few as one module and as many as 64. A complete line of cabinets is available to house the modules and their connector blocks, as well as providing a convenient means for system expansion. Power supplies for both large and small systems and reference supplies are also available.

Coupled with the recent additions to the hardware line, Digital has made every effort to maintain or improve the high standards of reliability and performance of its present line. Through the availability of a wide range of basic accessories. DEC feels that it is offering the logic designer the necessary building blocks which he requires for complete system design.

## 50-CYCLE POWER

Because of the demand for Digitals products in areas where 115-v, 60-cps power is not available, each of the power supplies with a frequency-sensitive regulating transformer is also available in a multi-voltage 50-cps version. All 50-cps supplies have the same input connections. The line input is on pins 3 and 4. Jumpers should be connected depending on the input voltage. These connections are shown below along with a schematic.

## WIRING HINTS

These suggestions may help reduce mounting panel wiring time. They are not intended to replace any special wiring instructions given on individual module data sheets or in application notes. For fastest and neatest wiring, the following order is recommended.

(1) All power & ground wiring and any horizontally bussed signal wiring. Use Horizontal Bussing Strips Type 932 or Type 933.

(2) Vertical grounding wires interconnecting each chassis ground with pin C grounds. Start these wires at the uppermost mounting panel and continue to the bottom panel. Space the wires 2 inches apart, so each of the chassis-ground pins is in line with one of them. Each vertical wire makes three connections at each mounting panel.

(3) All other ground wires. Always use the nearest pin C above the pin to be grounded, unless a special grounding pin has been provided in the module.

(4) All signal wires in any convenient order. Point-to-point wiring produces the shortest wire lengths, goes in the fastest, is easiest to trace and change, and generally results in better appearance and performance than cabled wiring. Point-to-point wiring is strongly urged.

The recommended wire size for use with the H800 mounting blocks and 1943 mounting panel is 24 for wire wrap, and 22 for soldering. The recommended size for use with H803 block and H911 mounting panel is #30 wire. Larger or smaller wire may be used depending on the number of connections to be made to each lug. Solid wire and a heat resistant spaghetti (Teflon) are easiest to use when soldering.

Adequate grounding is essential. In addition to the connection between mounting panels mentioned above, there must be continuity of grounds between

cabinets and between the logic assembly and any equipment with which the logic communicates.

When soldering is done on a mounting panel containing modules, a 6-v (transformer) soldering iron should be used. A 110-v soldering iron may damage the modules.

When wire wrapping is done on a mounting panel containing modules, steps must be taken to avoid voltage transients that can burn out transistors. A battery- or air-operated tool is preferred, but the filter built into some line-operated tools affords some protection.

Even with completely isolated tools, such as those operated by batteries or compressed air, a static charge can often build up and burn out semiconductors. In order to prevent damage, the wire wrap tool should be grounded except when all modules are removed from the mounting panel during wire wrapping.

## AUTOMATIC WIRING

Significant cost savings can be realized in quantity production if the newest automatic wiring techniques are utilized. Every user of FLIP CHIP modules benefits from the extensive investment in high-production machinery at Digital, but some can go a step further by taking advantage of programmed wiring for their FLIP CHIP digital systems.

While the break-even point for hand wiring versus programmed wiring depends upon many factors that are difficult to predict precisely, there are a few indications:

1. One-of-a-kind systems will probably not be economical with automatic wiring, even when the size is fairly large; programming and administrative costs are likely to outweigh savings due to lower costs in the wiring itself.

2. At the other end of the spectrum, production of 50 or 100 identical systems of almost any size would be worth automating, not only to lower the cost of the wiring itself but also to reduce human error. At this level of volume, machine-wired costs can be expected to be less than the cost of hand wiring.

3. For two to five systems of several thousand wires each, a decision on the basis of secondary factors will probably be necessary: ease of making changes, wiring lead time, reliability predictions, and availability of relevant skills are factors to consider.

The Gardner-Denver Corporation, and Digital can supply further information to those interested in programmed wiring techniques. At Digital, contact the Module Sales Manager, Sales Department.

## COOLING OF FLIP CHIP MODULES

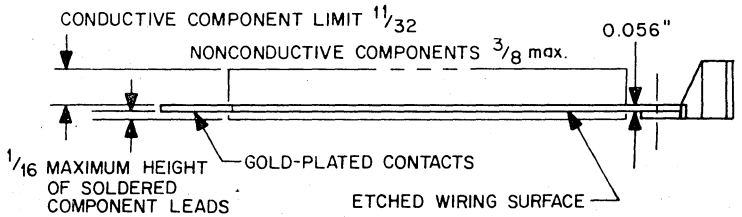
The low power consumption of K and M series modules results in a total of only about 25 watts dissipation in a typical 1943 Mounting Panel with 64 modules. This allows up to six panels of modules to be mounted together and cooled by convection alone, if air is allowed to circulate freely. In higher-dissipation systems using modules in significant quantities from the A series,

the number of mounting panels stacked together must be reduced without forced-air cooling. In general, total dissipation from all modules in a convection-cooled system should be 150 watts or less.

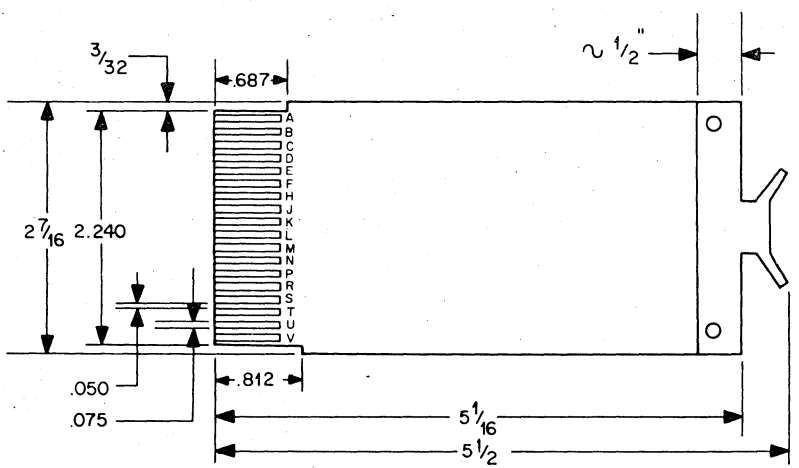
The regulating transformers used in most DEC power supplies have nearly constant heat dissipation for any loading within the ratings of the supply. Power dissipated within each supply will be roughly equal to half its maximum rated output power. If power supplies are mounted below any of the modules in a convection-cooled system, this dissipation must be included when checking against the 150 watt limit.

## STANDARD MODULE SIZES

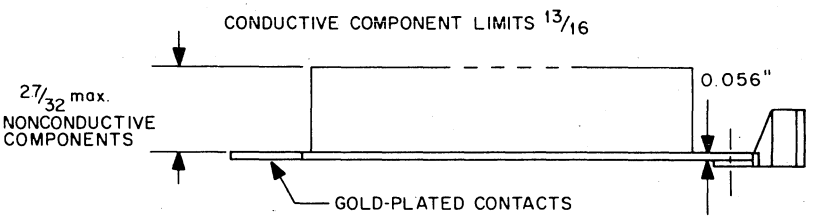
SINGLE-WIDTH FLIP CHIP MODULE



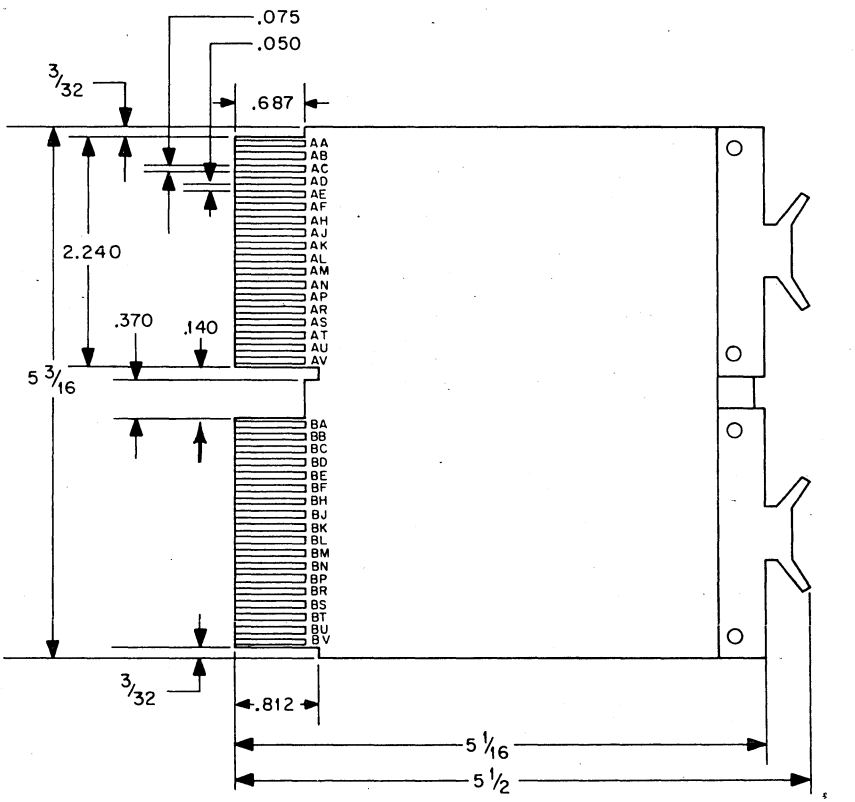

SINGLE-HEIGHT FLIP CHIP MODULE



DOUBLE-WIDTH FLIP CHIP MODULE

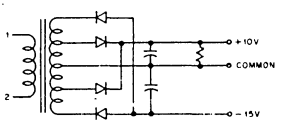



DOUBLE-HEIGHT FLIP CHIP MODULE



# POWER SUPPLIES
## H701, H701A, 782, 782A
## +10, −15 VOLTS

POWER SUPPLY




The 782 and 782A power supplies are ruggedly built, low cost units that fit into a standard 19-inch rack. The H701 and H701A are identical to these units, except they can be mounted on a chassis or panel in applications where space is added to an existing device. The basic supply can be mounted in various configurations and is identical to the power supplies used in models 700D and H900. The Types 782A and H701A are Power Supplies with 50 Hertz transformers.

### ELECTRICAL CHARACTERISTICS

**Input Voltage:** H701: 115 v 60 cps. H701A: 112.5, 123.5, 195, 220, 235 v, 50 cps. See "50 cps power"

**Output Voltage:** +10 v, −15 vdc, floating

**Output Current:** −15 v: ½ to 3 amp; +10 v: 0 to 0.4 amp.

**Line and Load Regulation:** The output voltage remains between −14.5 and −16.5 v for the −15 output, and within +9.2 and +11.5 v for the +10 output, when load varies from minimum to maximum and line voltage varies ±10%.

**P-P Ripple:** Less than 0.6 v for +10 output. Less than 0.6 v for −15 output; 20% more ripple on the 50-cps type.

**Line Frequency Tolerance:** ±2% of line frequency.

## MECHANICAL CHARACTERISTICS

**Height:** 5-3/4"

**Width:** 4-15/16"

**Length:** 8"

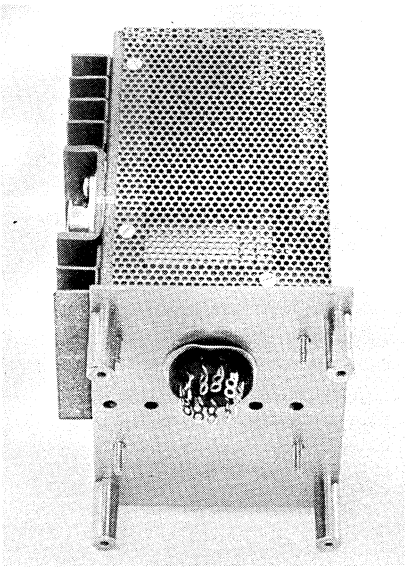
**Finish:** Chromicoat

**Power Connections:** Screw terminals are provided on transformer for input power conections. Output power connections are made via tab terminals which fit the AMP "Faston" receptacle series 250, part #41774 or Type 914 power jumpers. All required mounting hardware is supplied with this unit.

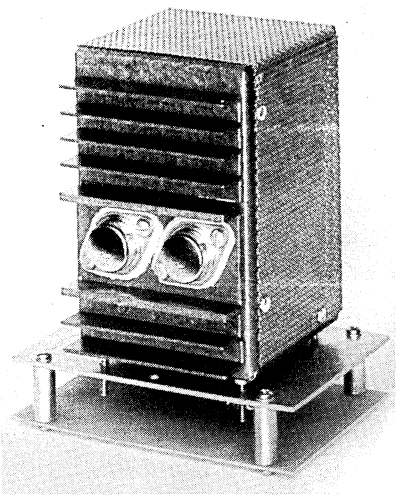
| | |
|---|---|
| H701 | — $116.00 |
| H701A | — $136.00 |
| 782 | — $128.00 |
| 782A | — $148.00 |

# DUAL POWER SUPPLY
## H704, H707
15 Volts

**POWER SUPPLY**



H704



H704

These supplies differ only in dimensions and output current capabilities: 400 ma and 1.5 Amperes respectively for the H704 and H707. May be mounted on the bars in an H920 drawer, taking the space of two connector blocks.

### MECHANICAL CHARACTERISTICS

DIMENSIONS: 3¼ x 3⅜ x 5 in. height (H704)
DIMENSIONS: 4" x 5" x 5½" height (H707)
CONNECTIONS: All input-output wires must be soldered to octal socket at the base of the power supply.
OPERATING TEMPERATURE: —20 to +71°C ambient

| |
|---|
| H704 — $200 |
| H707 — $400 |

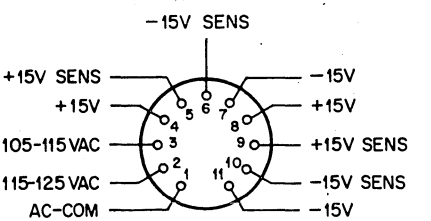
POWER CONNECTIONS:
Input power connections are made via tab terminals which fit the AMP "Faston" receptacle series. Output power is supplied to solder lugs. All required mounting hardware is supplied with this unit. See 914 power jumpers.

| | |
|---|---|
| Length: 8″ | Height: 6″ |
| Width: 5″ | Finish: Chromicoat |

## ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: 105 to 125 vac; 47-420 cps.
OUTPUT VOLTAGE: floating 15 v
OUTPUT VOLTAGE ADJUSTMENT: ±1 v each output
REGULATION: 0.05% line, 0.1% load for both voltages
RIPPLE: 1 mv rms max for both outputs
OVERLOAD PROTECTION: The power supply is capable of withstanding output short circuits indefinitely without being damaged.

IF REMOTE SENSING IS NOT USED, CONNECT: 5 TO 4
6 TO 7

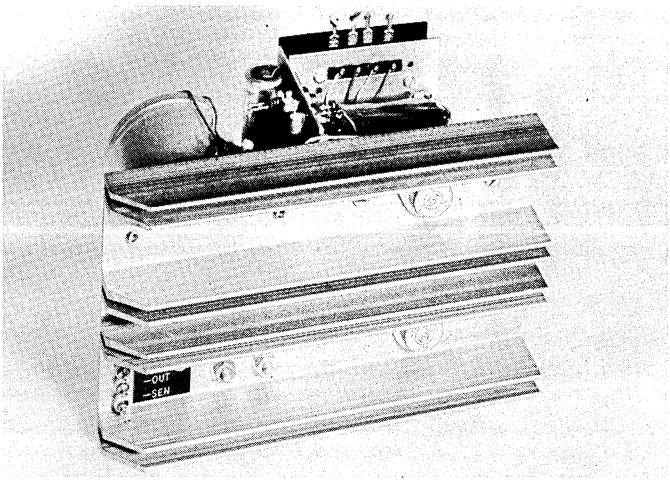



POWER SUPPLY 2

The H704 and H707 contain two 15 volt floating power supplies. To get ±15 volt supply, connect pins 7 and 8 and use this point as ground. Pin 4 will now be at positive 15 volts and pin 11 will be negative 15 volts.

# POWER SUPPLY
## H710

POWER SUPPLY




The H710 power supply is ruggedly built, low cost, regulated, floating output, five volt power supply that can be mounted in an H920 chassis drawer or used as a free standing unit.

| INPUT VOLTAGE: 105-125 VAC or 210-250 VAC 47-63 HZ | OUTPUT VOLTAGE: 5 vdc. | P-P RIPPLE Less than 20 mv. |
|---|---|---|

OUTPUT CURRENT:
0-5 amps, short-circuit protected for parallel supply operation.

LINE AND LOAD REGULATION:
The output voltage will not vary more than 50 mv. over the full range of load current and line voltage.

REMOTE SENSING:
Remote sensing is provided to correct for loss due to long lines. These sensing inputs should be connected to the most distant point on the +5 and ground buss system. When shipped from the factory, the remote sensing inputs are jumpered to their respective outputs. These leads are especially useful in systems that require maximum repeatability from K303 timers in the millisecond region.

OVERVOLTAGE PROTECTION:
The output is protected from transients which exceed 6.9 volts for more than 10 nsec. However, the output is not protected against long shorts to voltages above 6.9 volts.

H710 — $200

# POWER SUPPLY
## H716

POWER SUPPLY

Type H716 provides +5 volts at 4 amperes and —15 volts at 1.5 amperes with over voltage protection for +5 volts. This dual voltage power supply is designed to be mounted at the right end of any mounting panel which incorporates the Type H021 mounting frame. The supply is mounted by using the four holes in the Type H021, therefore the right end plate cannot be used when a Type H716 supply is mounted. The supply takes 2 connector blocks of Type H800, H803, or H808. This provides 48 module slots with Types H800 and H803, 24 slots with Types H800 and H803 and 24 slots when Type 808 is used.

### MECHANICAL CHARACTERISTICS

Maximum Dimensions 5¼ x 4⅛ x 12 deep

Power input via Amphenol 160-5 or equivalent connector with an Amphenol 160-5 or equivalent, in parallel.

Low voltage connections are by slip on terminals.

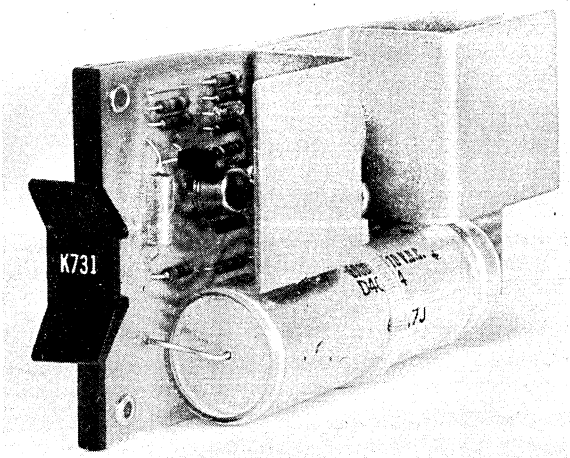
### ELECTRICAL SPECIFICATIONS

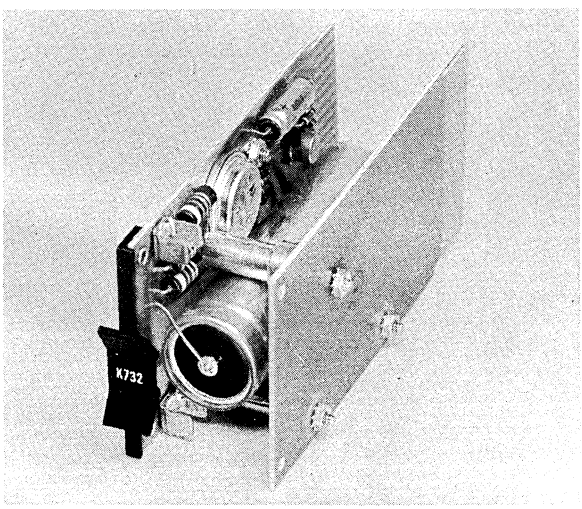
| | |
|---|---|
| Input: | 120/240 vac ± 10%, 47-63 HZ. Normally supplied wired for 120v. For 240 volts change transformer tap connections. |
| Output 1: | +5v, adjustable from 4.5 to 5.5 volts at 4 amperes maximum. Line-Load-Ripple total regulation ±3%. |
| Output 2: | —15v ±5% at 1.5 amperes, maximum. Line-Load-Ripple total regulation ±5%. |
| Temp. Range: | Above specifications are over a range of 0-50°C. |

H716 — $130

# POWER SOURCE MODULE
## K731
# SLAVE REGULATOR
## K732

POWER SUPPLY



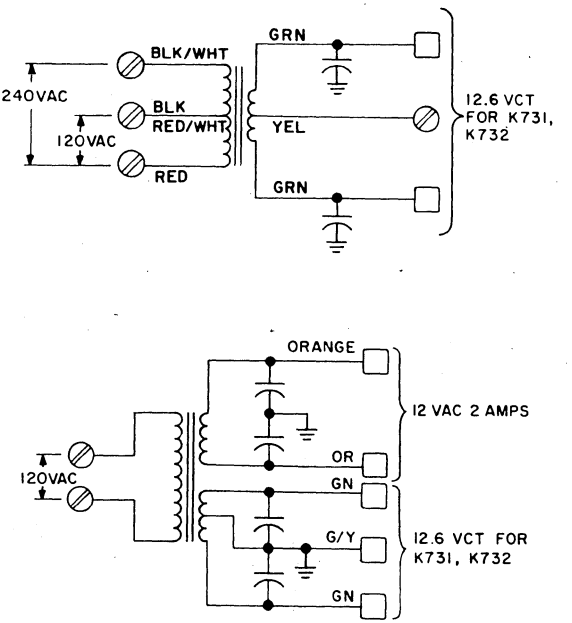




One K731 plus up to 3 K732 can provide from 1 to 7 amperes at +5v. Consult K Series text for additional characteristics and hook up information.

K731 — $30
K732 — $27

# POWER TRANSFORMERS
## K741, K743

**POWER SUPPLY**

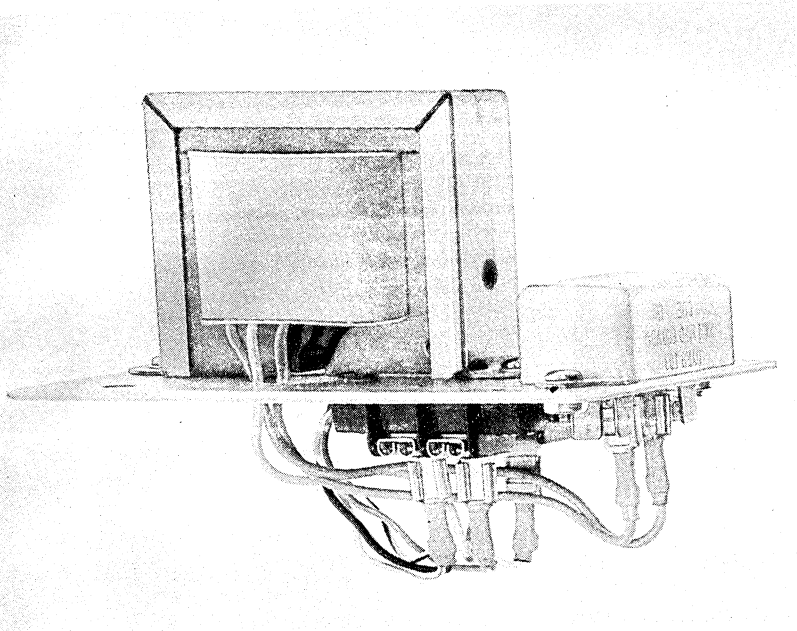



These hash-filtered, 50/60 Hz transformers supply K731 Source and K732 Slave Regulator modules. The K743 also provides an auxiliary winding for use with K580 Dry Contact Filters, K681 or K683 Lamp Drivers (requires additional bridge rectifier, and the K730 Supply and Control Module. Type 914 Power Jumpers are convenient for connecting to tab terminals on these transformers and on the K732 and K943. Both transformers have holes at the corners of the chassis plate for mounting on K980 endplates:

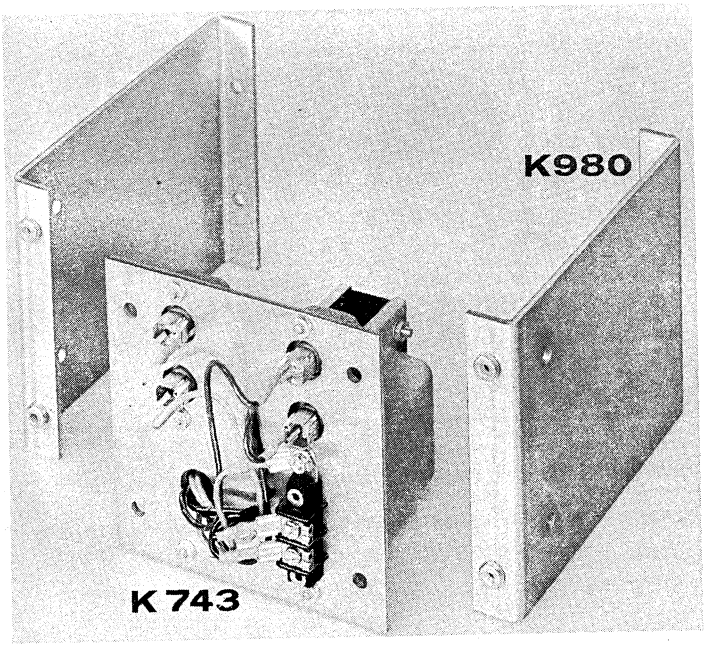
| | PLATE DIMENSIONS | HOLE CENTERS | MATCHING K980 Ctrs. |
|---|---|---|---|
| K741 | 3½" x 5" | 2½" x 3⅜" | 2½" |
| K743 | 5" x 5" | 4" x 3⅜" | 4" |

The K741 is sufficiently light in weight to be mounted on one side only, as at the end of a K943 mounting panel.

K741 — $30
K743 — $45



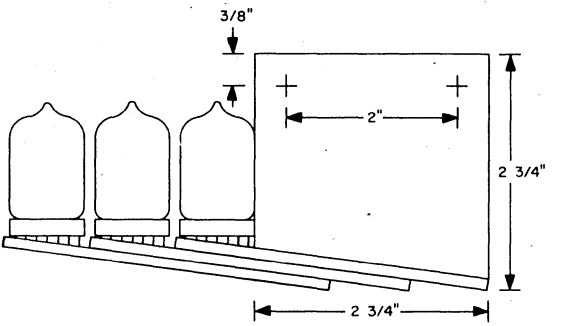
K741




K743

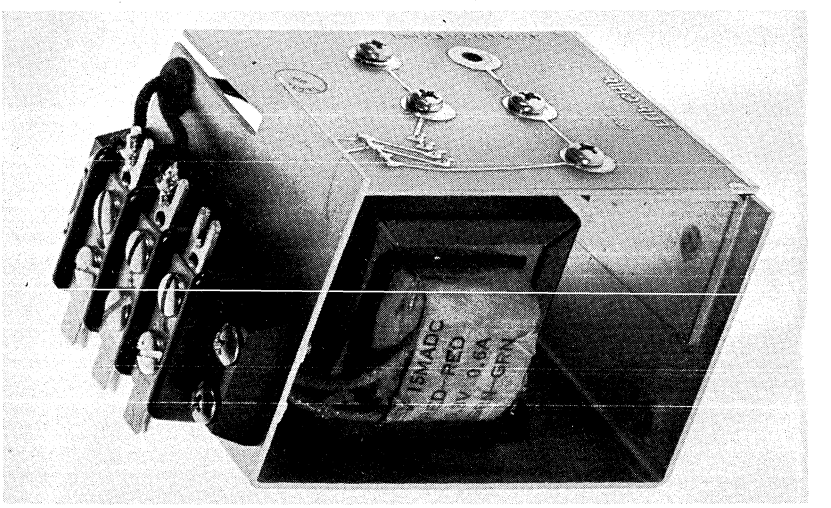
# DISPLAY SUPPLY
## K771

**POWER SUPPLY**



(SHOWN WITH 3 K671'S).

Shown above from the viewing side, the K771 supplies power and a convenient two-screw mounting for up to 6 K671 display tubes. Display tubes are stacked to the left, the first tube board being attached to the K771. The second tube board attaches to the first, and so on. Board mounting screws provide both mechanical mounting and electrical power connections. The two panel mounting screw locations dimensioned above have No. 6 steel threaded inserts. Several 1″ holes using a standard chassis punch may be cut on 0.8″ centers for viewing display tubes. To seal opening against dust, a 3″ by 3-6″ piece of Lucite® or Plexiglas® may be assembled between display and mounting surface. Power 120 VAC enters the supply from a terminal strip at the rear. Total depth behind mounting surface: 4″.



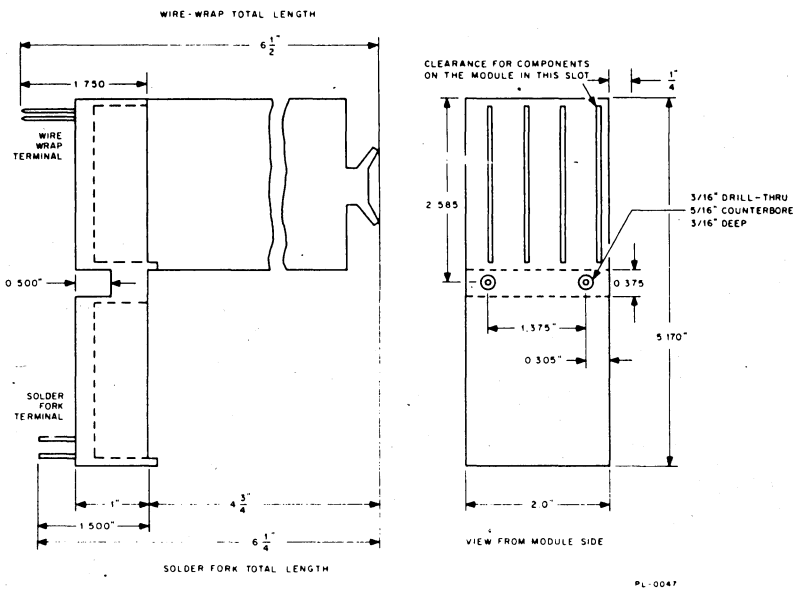
K771 — $35

# CONNECTOR BLOCKS
## H800-W, H800-F

**UNIVERSAL HARDWARE**

This is the 8-module socket assembly used in Flip-Chip mounting panels. Because of its 18 pin connectors, it can be used for all modules except those with pins on both sides of the board. Pin dimensions are .031 inches by .062 inches and may be of either a wire wrap or solder fork type. Number 24 wire should be used with these connectors.

The drawings below show the pertinent dimensions.




### REPLACEMENT CONTACTS TYPES H801-W, H801-F

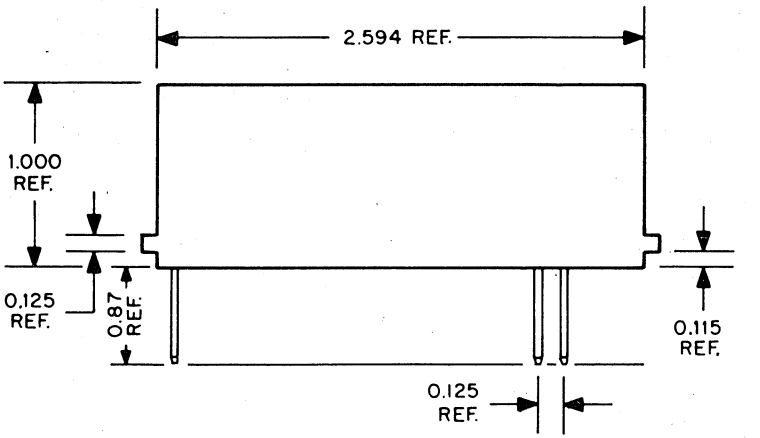
These contacts are offered in packages of 18 for replacement purposes. In each package, nine straight and nine offset contacts are included, enough to replace all contacts in one socket.

H801-W is for wire-wrap connectors; H801-F is for solder-fork connectors.

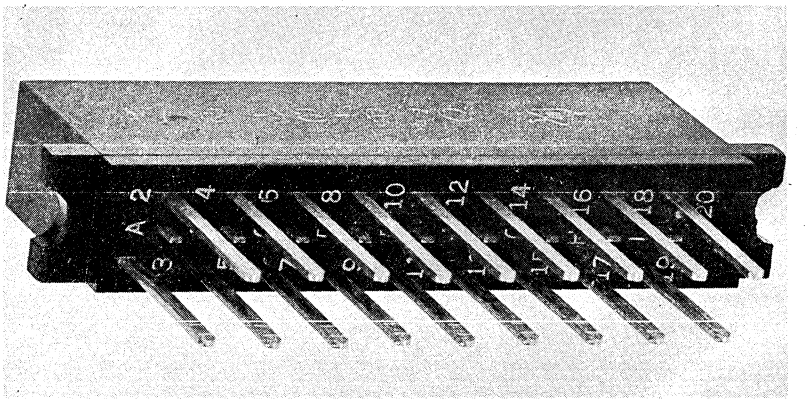
| | |
|---|---|
| H800F | $8 |
| H800W | $8 |
| H801F | $2 |
| H801W | $2 |

# CONNECTOR BLOCK
H802

UNIVERSAL HARDWARE



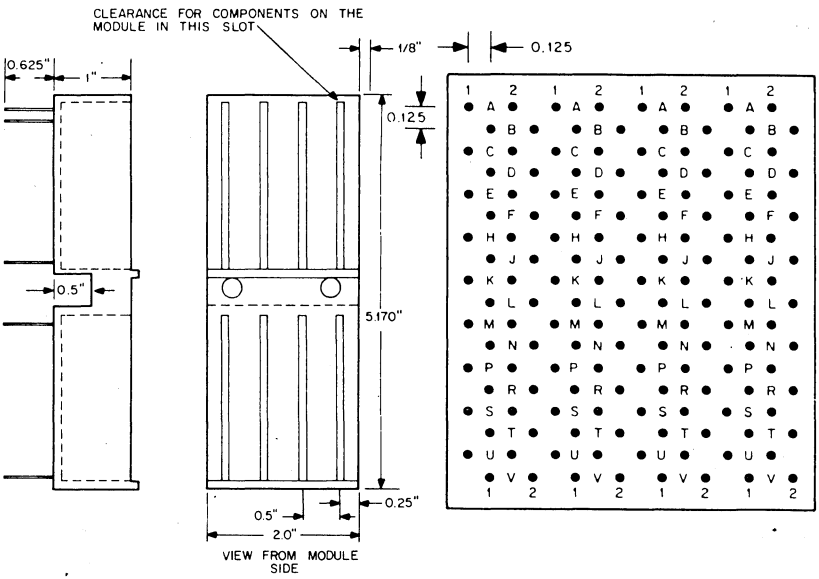

This is an 18 pin connector block for a single FLIP CHIP module. It can be used to mount all modules except those with pins on both sides of the board. Pin dimensions are .031 inches by .062 inches and may be of the wire wrap type only. Number 24 wire should be used with this connector.



H802 — $4

# CONNECTOR BLOCK
## H803, AND H805 PINS

**UNIVERSAL HARDWARE**




The H803 is the 8-module molded Jacket Assembly used in the H910 and H911 mounting panels. For each of the eight modules, it provides a 36-pin connector with the wirewrap pins forming a 0.125-inch staggered grid as shown above. This connector is designed to be used with M Series modules; however, it can also be used with all other series listed in this handbook.

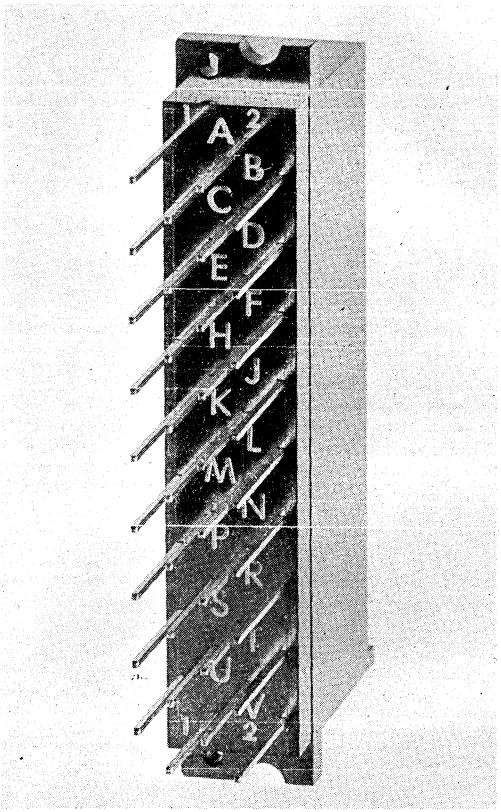
The blocks have the same physical dimensions as the H800 with the exception of pin length. These blocks are only available with wire wrap pins which are designed to be wrapped with number 30 wire. Pin dimensions are 0.025 inches square. W&K Series 18 pin modules will make contact with only the 2-side pins (A2, B2, etc.).

H805 is a package of 36 pins (18 left and 18 right) to be used as replacements in H803 blocks. Three types are available depending on the manufacturer of Type H803 whose name or symbol is found on the connector mounting block.

H803 — $13
H805 — $4

# CONNECTOR BLOCK
H807

UNIVERSAL HARDWARE

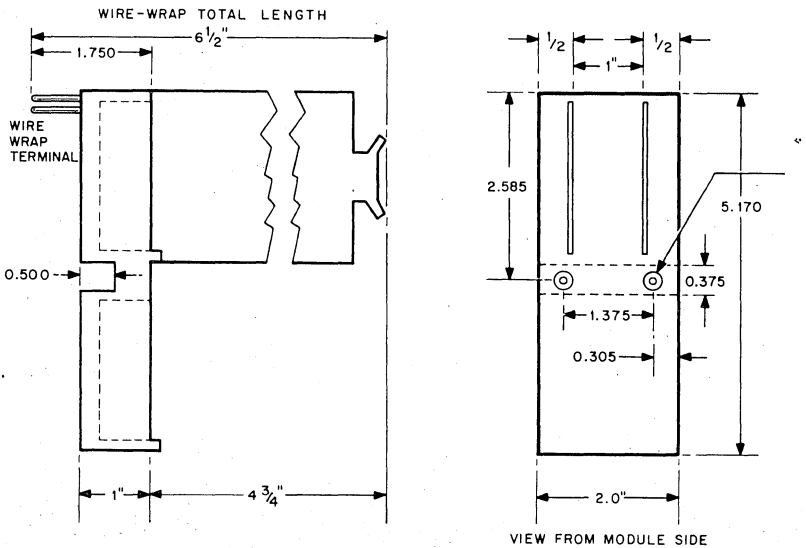



This is a 36 pin single slot connector. It is provided for M-Series modules but can be used with modules or connector boards in the K and W Series. Uses include mounting in confined or irregular spaces. Often the H807 is used to terminate a connector board at a remote location. The H807 is available only with wire wrap pins. Number 30 wire should be used with this connector.

H807 — $5

# CONNECTOR BLOCK
## H808, H809 PINS

**UNIVERSAL HARDWARE**




The H808 is a relatively low density connector block for use with all modules in the catalog. This includes A, K, M, and W Series modules. The connector provides 4 module slots each having 36 pins. On A, K and W Series modules only the 2 side pins, (A2, B2, etc.) will make contact. This connector adds a measure of convenience and versatility to the many uses to which these catalog modules can be applied. The dimensions of the connector pins are the same as those for the H800 (.031 inches by .062 inches). Number 24 wire should be used with these blocks, H800 and H808 connector blocks can be mixed for M and A, K, W module mixing purposes. Wire wrapping patterns can be maintained even though module letter series are mixed because H800 and H808 pin layout is identical. H809 is a package of 36 replacement pins, 18 left and 18 right.

H808—$10
H809—$ 4

# MOUNTING PANEL HARDWARE
## H001, H002, H020, H021, H022

**UNIVERSAL HARDWARE**

**PAIRS OF SETBACK BRACKET:**

H001 — ¾" standoff used to mount a 1907 over K943 wiring as shown in the description of the K943.

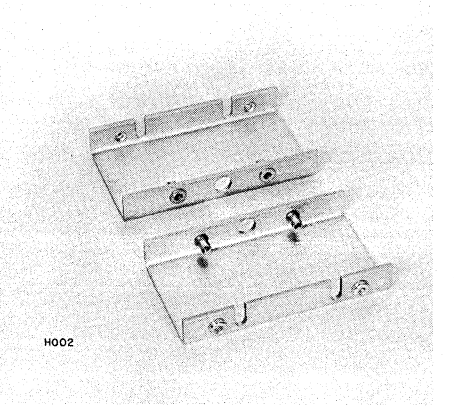
H002 — 2" setback-used to mount a control panel with switches, lamps, etc. This setback brings the control panel up flush with the mounting rack or cabinet in front of the logic wiring.

**MOUNTING FRAMES**

H020 — Mounting frame casting upon which H800, H803, H808 connector blocks, power supplies, such as, the H710 and other components that are adaptable to the frame mounting requirements can be mounted.

H021 — Single offset end plate which mounts to the H020. This end plate provides a mount for the 1945-19 hold down bar, if required.

H022 — Single end plate similar to the H021 on which is mounted a terminal block assembly for ease of parallel power wiring to adjacent panels.

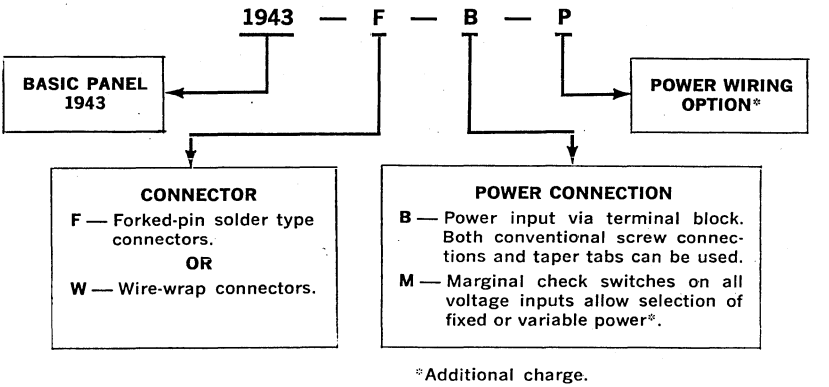



H001-PR — $8
H002-PR — $8
H020 — $15
H021 — $7
H022 — $20

TYPE 1943 MOUNTING PANEL

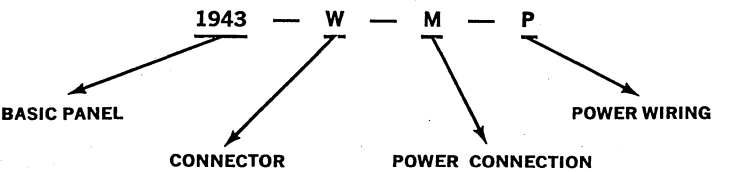
The 1943 Mounting Panel houses 64 modules. It is designed for mounting in a standard 19-in. rack. The mounting panel is finished with an aluminum conversion coating (Chromicoat). Filter capacitors are included on all power supply lines.

Available options are solder or wire-wrap connectors, power input via terminal strip or marginal check switches, and power wiring. The chart below shows how the options are indicated when ordering.




*Additional charge.

EXAMPLE: If you require a Type 1943 Mounting Panel with wire-wrap connectors, marginal check switches on the power connection, and prewired power, you would order:



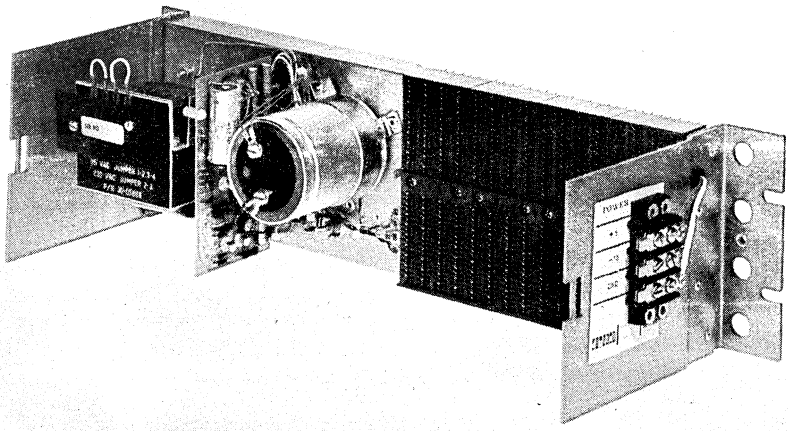

MECHANICAL DIMENSIONS: 19 in. wide; 5-3/16 in. high; 6-3/4 in. deep. Tabs for power connections fit AMP "Faston" receptacles, series 250, part 41774 or Type 914 power jumpers.

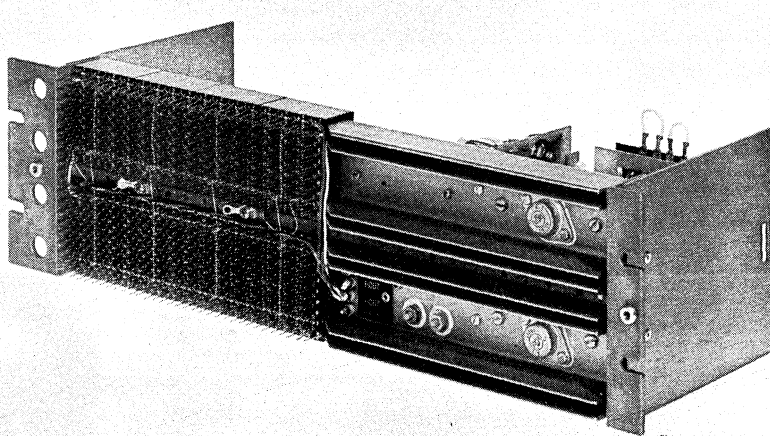
1945-19 HOLD DOWN BAR: Reduces vibration and keeps modules securely mounted when panel or system is moved. Adds 1/2 in. to depth of mounting panel.

| | |
|---|---|
| 1943-F-B | — $111.00 |
| 1943-W-B | — $111.00 |
| 1943-F-B-P | — $121.00 |
| 1943-W-B-P | — $121.00 |
| 1943-F-M | — $132.00 |
| 1943-W-M | — $132.00 |
| 1943-F-M-P | — $142.00 |
| 1943-W-M-P | — $142.00 |
| 1945-19 | — $ 15.00 |

# MOUNTING PANEL
H910

UNIVERSAL HARDWARE





The dual function mounting panel offers a way to build complete digital systems of up to 32 FLIP CHIP modules into only 5¼ inches of rack space. More power is available than is ever likely to be consumed in a 32 module system. Power in excess of that required for modules can be obtained at the H022 terminal block which is conveniently located for connection to the input H022 terminal block on any adjacent H911 or 1943 mounting panel.

The H910 panels are built from four H803 connector blocks and a 5 volt regulated supply. Wire wrap connectors for 30 awg wire only are present on the H910. The panel will hold 32, 36 pin modules. In addition, the panel is bussed with 933 bus strips on pins A2, C2, and T1 and all power wiring to the supply is connected. Power in excess of that required for the 32 modules can be obtained at the terminal block which is convenient to the input terminal block on any adjacent H911 mounting panel, generally used for M series modules.

## ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE:
105-125 VAC or 210-250 VAC
47-63 HZ
OUTPUT VOLTAGE:
5vdc

OUTPUT CURRENT:
0-5 amps. short-circuit protected for parallel supply operation

OVERVOLTAGE PROTECTION:
The output is protected from transients which exceed 6.9 volts for more than 10 nsec. However, the output is not protected against long shorts to voltages above 6.9 volts.

## MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5$\frac{3}{16}$ in.
DEPTH: 16¾ in.
FINISH: Chromicoat
POWER INPUT CONNECTIONS:
Screw terminals

vided on transformer
MODULES ACCOMMODATED: 32
POWER OUTPUT CONNECTIONS:
Barrier strip with screw terminals and tabs which fit AMP "Faston" receptacle series 250, part no. 41774 or Type 914 power jumpers.

H910 — $280

# MOUNTING PANEL
## H911-J, H911-K

**UNIVERSAL HARDWARE**

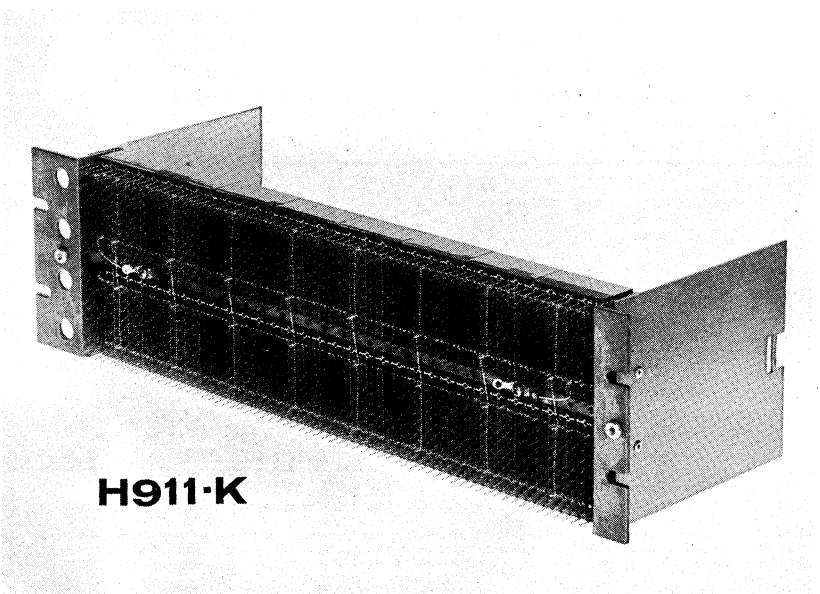
The H911 mounting panel uses eight H803 connector blocks and houses sixty four, 36 pin connectors. Mechanical dimensions are identical to those of the H910.

The H911 is available with wire wrap pins only, and is generally used for M Series modules.

The unit is a combination of the following parts:

H020 — Mounting frame
H021 — Standoffs
H803 — Connector blocks
933 — Bussing strips (optional with H022 standoff)

The H911J is not prewired or bussed for power.
The H911K does have prewired power.




933 BUS STRIP — For H911 mounting panel, makes wiring power and register pulse busses easy.

Consult following table for option and ordering information.

| |
|---|
| H911J — $151 |
| H911K — $161 |

# MOUNTING PANEL
## H913, H914, H916 & H917

**UNIVERSAL HARDWARE**

H913 — This panel houses a 5v regulated supply and four low density H808 connector blocks. This allows 16 of either A, K, M, or W Series modules to be used. Electrical and mechanical characteristics are like those of type H910.

H914 — This panel houses 8 low density H808 connector blocks. The panel will hold 32 of either A, K, M or W Series modules. It can be used for expanding slot capacity in conjunction with H913 or alone using other voltage supply options, e. g. K731 and K732 combinations. Mechanical characteristics are like those of the H911.

H916 — This panel contains an H716 power supply and 6 H803 (green) connector blocks. The unit provides for forty-eight, 36 pin module slots. Although generally used for mixes of M and A series modules, K and W series modules can also be accommodated.

H917 — This panel is similar to the H916 panel except 6 low density H808 connector blocks are supplied instead of H803 blocks. With these connector blocks, 24 module slots are available, allowing the use of any module series. Electrical and mechanical characteristics are similar to those of type H916 with the exception of the connector blocks.

| | |
|---|---|
| H913 | $270 |
| H914 | $125 |
| H916 | $270 |
| H917 | $260 |

## TABLE OF MOUNTING PANELS WITH & WITHOUT POWER SUPPLY

| ORDER NO. | | AVAILABLE VARIATIONS | | | | | | PRICE |
|---|---|---|---|---|---|---|---|---|
| PANEL | ORDER LETTER | X | V | F | W | B | P | |
| H910 | K | | * | | * | * | * | $280 |
| H911 | J | * | | | * | * | | $151 |
| H911 | K | * | | | * | * | * | $161 |
| H913 | L | | * | | * | * | * | $270 |
| H914 | L | * | | | * | * | | $125 |
| H916 | M | | * | | * | * | * | $270 |
| H917 | N | | * | | * | * | * | $260 |
| K943 | R | * | | * | | | * | $ 96 |
| K943 | S | * | | | * | | * | $ 96 |

**X** = NO POWER
**V** = POWER OPTION
105-125 VAC OR
210-250 VAC
47-63 Hz

**P** — PREWIRED FOR POWER

**F** — SOLDER FORKED CONNECTIONS
**W** — WIRE WRAP CONNECTIONS

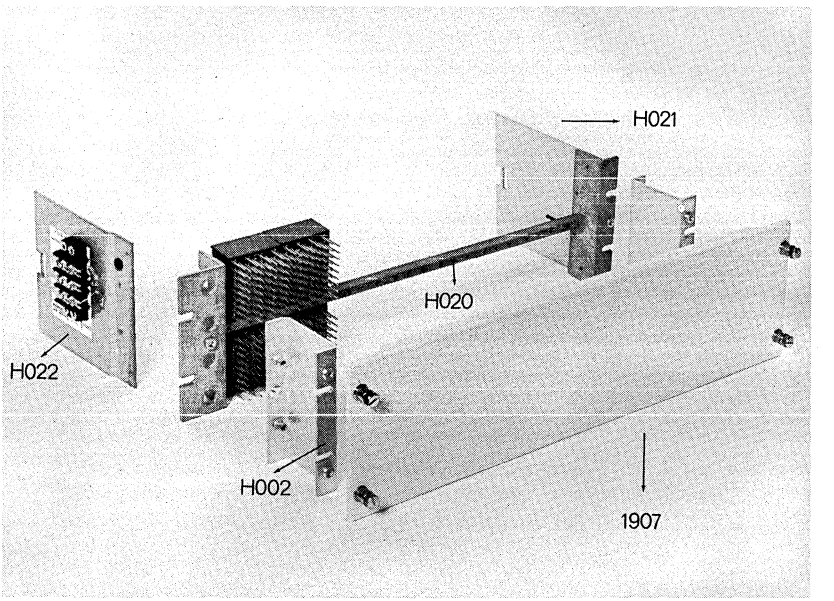
**B** — POWER INPUT VIA TERMINAL BLOCK. BOTH CONVENTIONAL SCREW CONNECTIONS AND TAPER TABS CAN BE USED

Example Order: H911KX
This describes a Type H020 casting with 8 Type H803 wire wrap connectors and ground wired to a terminal block incorporated into the end plate assembly.

# COVER
## 1907

**UNIVERSAL HARDWARE**

Blue painted or brown tweed painted aluminum cover with captive screws to mate threaded bushings in K980 and H001. Adds to appearance while protecting system against vibration and tampering.




1907 — $9

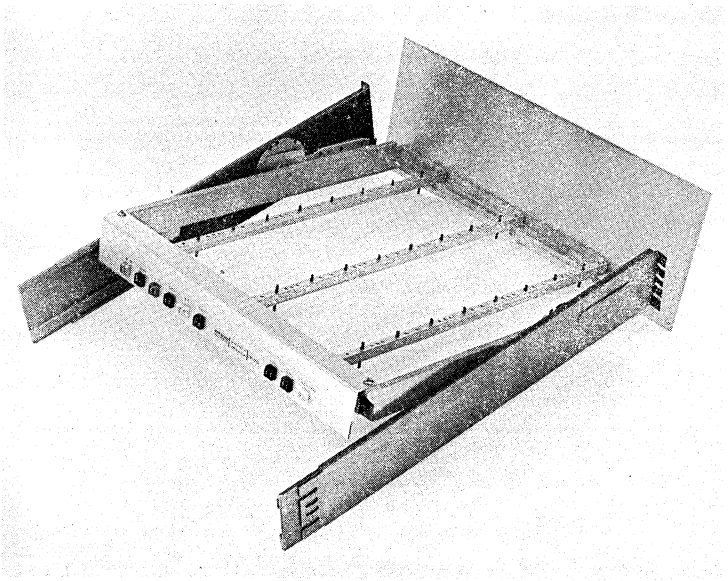
# MODULE DRAWER
## H920

UNIVERSAL HARDWARE

The H920 Module Drawer provides a convenient mounting arrangement for a complete digital logic system. The H920 has space for 20 mounting blocks in addition to an H710, or H716 power supply, or 24 mounting blocks without a supply. It accepts H800, H803, and H808 mounting blocks and fits standard 19″ racks. Width of the H920 is 16¾″, depth is 19″ and height is 6¾″ including an H921 front panel. The H920 is equipped with a bracket for distributing power within the drawer, or to other drawers or mounting panels. Mounting arrangements are provided for the H921 front panel and H923 slide tracks.

The H921 front panel is designed for use primarily with the H920 Module Drawer. It provides mounting space for switches, indicators, etc. The H921 is pre-drilled and ready to mount on the H920. Height of the H921 is 6¾″, width is 19″.

H923 chassis slides are intended for use with the H920 Module Drawer. The H923 allows the user to slide the drawer out of the rack and tilt the drawer for easy access.



H920 — $170
H921 — $ 10
H923 — $ 75

# MODULE DRAWER
## H925

UNIVERSAL HARDWARE

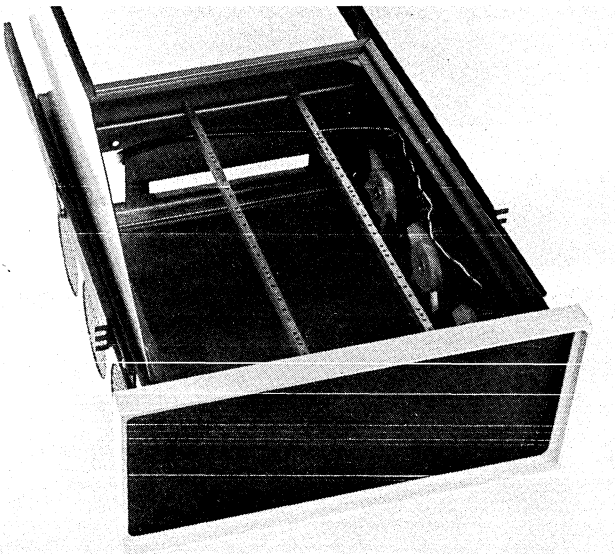
The H925 Module Drawer provides mounting space for H800, H803, and H808 connector blocks to accommodate up to 144 modules. The connector blocks mount pins upward on the H925 for easy access during system checkout.

The right side of the H925 is provided with three axial flow fans (300 cfm) which are mounted internally. They provide cooling air flow across the mounted modules.

For power supply mounting in the H925 cabinet, omit 4 connector blocks thereby deleting 32 module slots, when using the H800 or H803 connector blocks. If the H808 blocks are used, 16 module slots are deleted. Mount the power supply externally if all logic mounting space is required.

For ease of mounting, the H925 is provided with two non-tilting slides, similar to Grant type SS-168-NT. Considering possible servicing, the H925 should be mounted with enough height for using bottom access.

The H925 includes top and bottom cover plates along with an attractive bezel and front subpanel. The subpanel is made of sturdy 16-gauge metal for mounting front panel controls and accessories. The bezel is designed for installing a customer-supplied dress panel. The dress panel should have a thickness of $\frac{1}{8}$". The H925 fits all DEC 19" racks.



H925 — $250

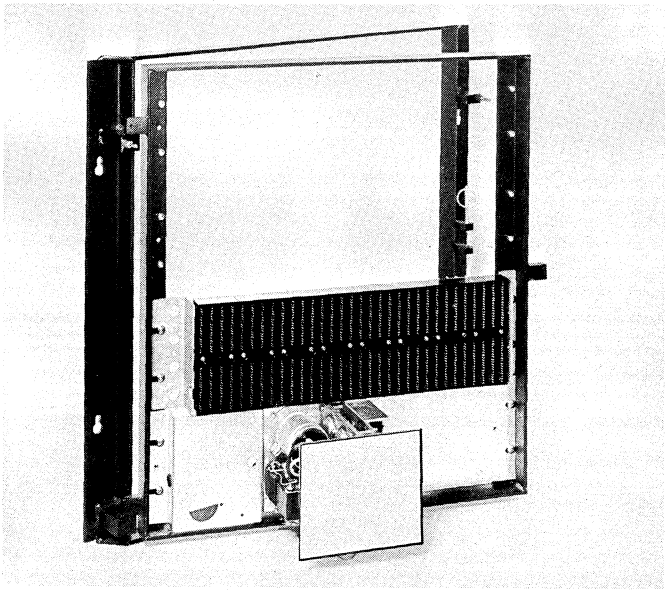
# 19″ MOUNTING PANEL FRAME
## H941AA

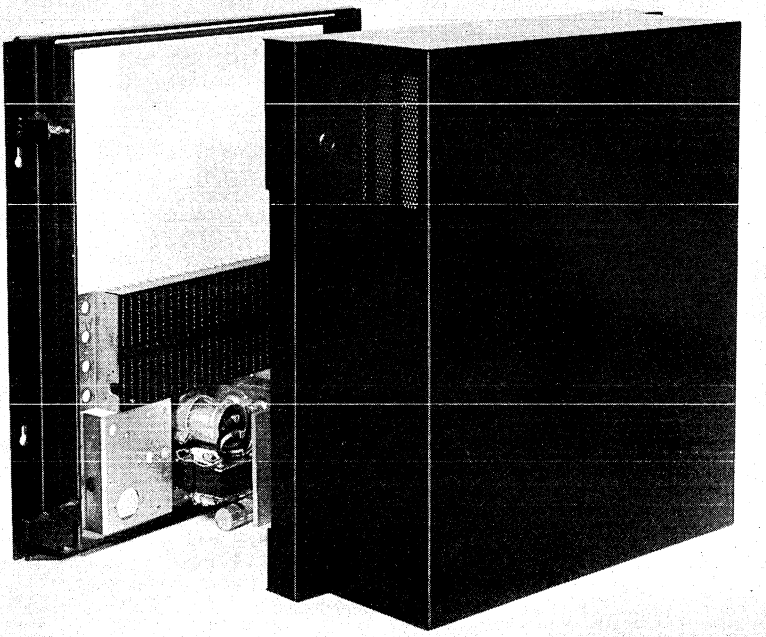
**UNIVERSAL HARDWARE**

This rugged steel frame holds four 19″ x 5¼″ mounting panels. A quick-release pin snaps out to allow the two-piece frame to swing open for easy access to the back panel wiring and connections. The construction of this frame allows sufficient rigidity for vertical or horizontal mounting. The Black Tweed finished aluminum cover affords mechanical protection for the circuitry as well as a neatly finished appearance for your digital logic system. The cover attaches to the frame with two thumb-release, positive-grip fasteners.

The H941 AA holds up to 32 H800, H803 and H808 Connector Blocks. It provides up to 256 module slots with H800 and H803 Connector Blocks and 128 slots with the H808's. The frame is designed to accept K943, H911, H914, 1943 Module Panels and H900, H910, H913, H916, H917 panels with power supplies. These panels attach to the pre-tapped frame with 10-32 x ½″ machine screws.

Frame Height: 23″
Frame Width: 24″
Overall Depth (Cover and Frame): 8″
Frame Mounting Hole Centers: 12 x 22½″
Frame Mounting Bolt: ¼″ dia.
Weight (Cover and Frame): Approx. 25 lbs.
Cover Material: .093″ Sheet Aluminum

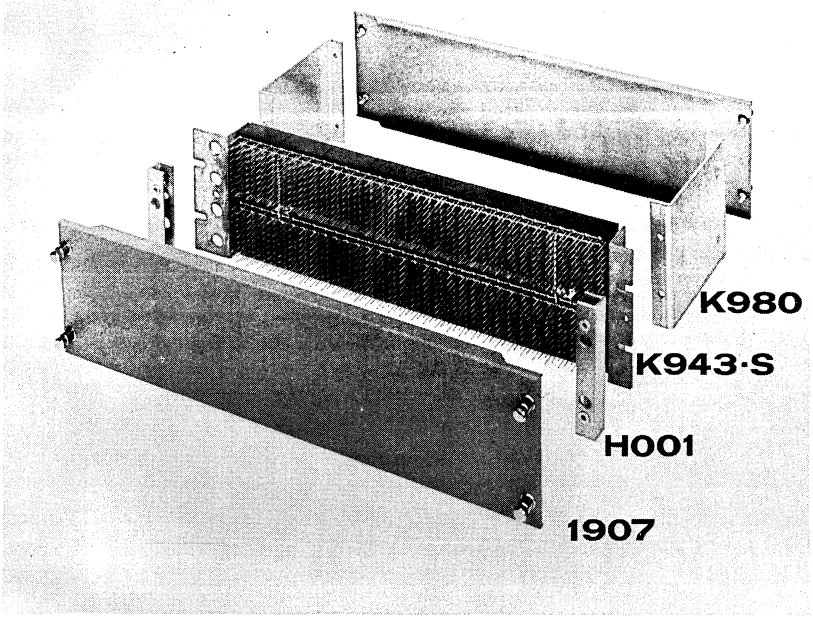




H941 BA, H941 AA
Includes Cover and
Two Piece Frame
$175.00

# 19″ MOUNTING PANEL
K943-R, K943-S

UNIVERSAL HARDWARE



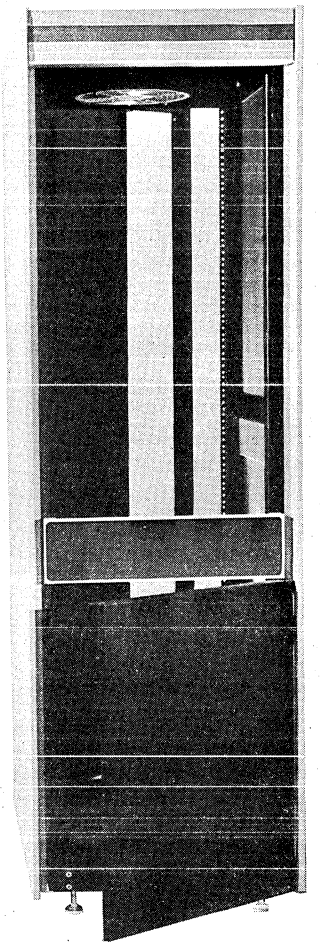

These low cost, 19″ panels have sixty four, 18 pin connector sockets with either wire-wrap (R) or solder fork (S) contact pins. Shipped with connector blocks installed and pins A and C bussed.

No terminal strips are included in the K943, since power regulators K731 and K732 will normally be plugged in to make power connections. If hold-down is required to prevent modules from backing out under vibration, order a pair of end plates K980. These assemble by means of added nuts on the rear of the rack mount screws. They accept the painted 1907 cover plate, making a hold-down system that contacts the module handles and can allow flexprint cables to be threaded neatly out the end. Rack space: 5¼″. See photos showing K943-S, K980, 1907, and H001.

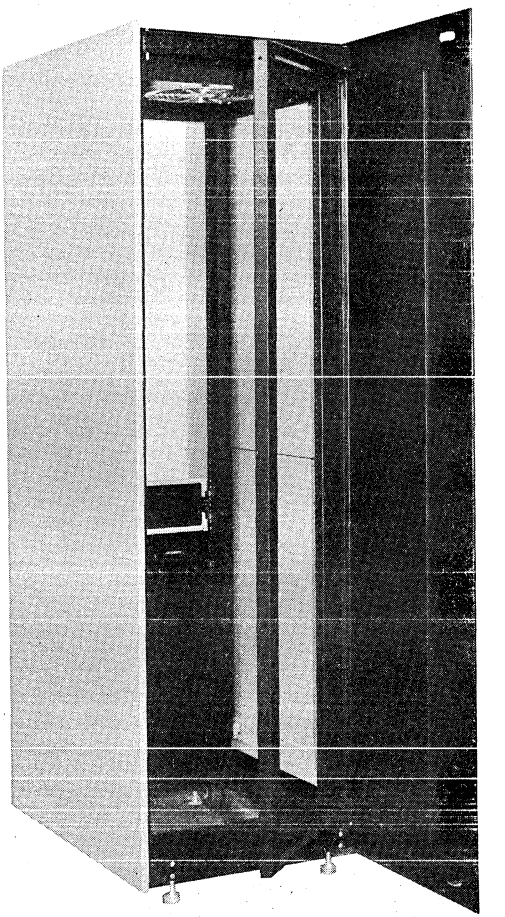
K943R — $96
K943S — $96

# CABINET
## H950

UNIVERSAL HARDWARE



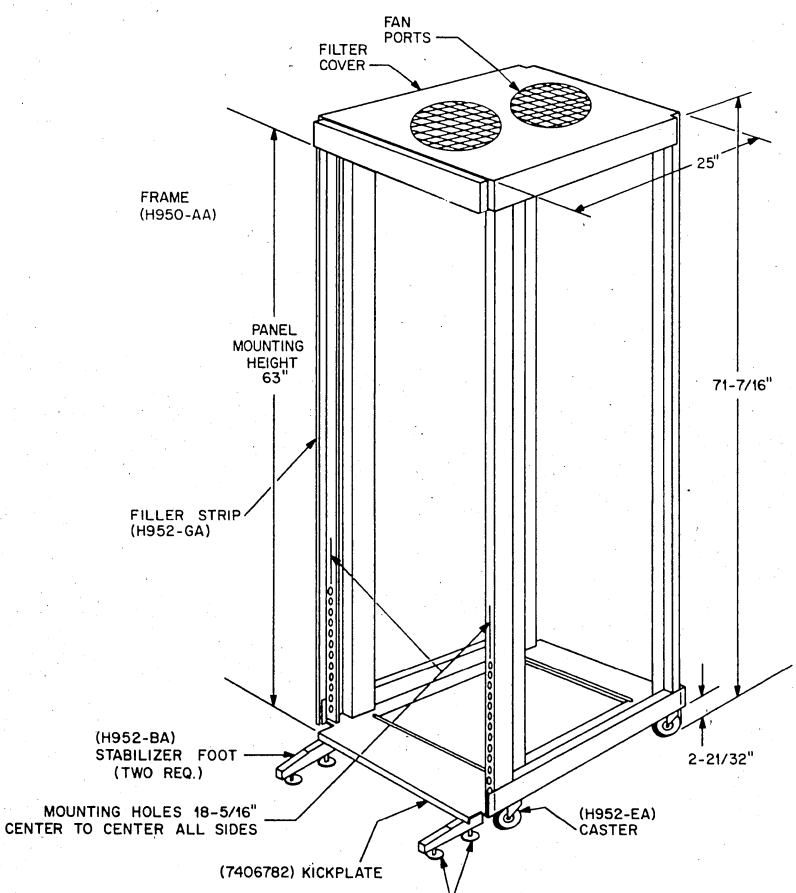
Front view of H950 frame.



Rear view of H950 frame.

Digital Equipment Corporation manufactures a standard 19″ mounting frame assembly that offers the customer complete flexibility in selecting hardware to design the cabinet. It is a complete enclosure designed to house module racks, power supplies, computer, systems, and peripherals.

The H950-AA frame assembly, which includes a filter cover, is designed for sophisticated computer systems. It is constructed of rugged 12 and 13 gauge steel. The two pairs of frame uprights have 9/32″ holes drilled at standard EIA spacings (5/8 — 5/8 — 1/2) the full length of the 63″ mounting panel height.



# OPTIONAL PARTS
## H950

UNIVERSAL HARDWARE

1. The H952-EA caster set (4) and H952-FA leveler set (4) are needed for the H950 frame to provide mobility and balance to the cabinet.
2. The fan assembly H952-CA is mounted to the top pan of the H950-AA frame. When ordering, please specify the direction of air flow, up or down.
3. H952-AA end panels are standard gray and are easily mounted to the frame.
4. The frame identification panel (LOGO) H950-LA is available with colored adhesive inlay strips of brown/yellow or dark blue/light blue.
5. The H950-P or -Q bezel cover panel is available in heights of 5¼" and 10½" with a 19" panel width. It is used as a cover panel or filler for the front of the cabinet. The customer can select any combination of bezels to fill the cabinet's front panel space of 63".
6. The H950-HA through H950-HK series of short doors is available for mounting to the cabinet's front side. A various table of short doors is listed in the H950 parts list. The customer has the option of completing the front side of the cabinet with a combination of short doors and bezels. NOTE: Dimensions of doors listed only cover mounting panel height. Check special considerations section for short door limitations.
7. The H950-BA (right-hand door) and H-950-CA (left-hand door) are full doors for rear and front mounting to the H-950-AA frame. See special considerations section for front mounting.
8. The rear mounting panel door, also called a plenum door H950-DA or EA, is for left-hand or right-hand mounting. There is a distinct advantage to using the plenum door for mounting power supplies, logic racks, module connector block panels, etc. It offers convenient access for servicing and mounting equipment. It is designed for 19" panels and holes are drilled to 9/32" at standard EIA spacings (⅝—⅝—½) the full length of the plenum door frame. The customer has the option of selecting a rear mounting panel door skin H950-FA that bolts to the plenum door or ordering a full door. For additional information, see special consideration section.
9. The filter H950-SA should be ordered only for fans that are to be used for air flow intake.

**Special Considerations**
Before ordering a cabinet, the following should be considered:

1) If a LOGO is used, only a short door can be used on the cabinet front.

2) When ordering a cabinet to add to a system, or when joining two or more cabinets, front and rear fillers H952-G are required.

3) If power supplies with meters or switches are mounted to the plenum door H950-DA (RH) or H950-EA (LH), a full door H950-DA (RH) or H950-CA (LH) is needed.

4) The mounting panel door skin H950-FA bolts to the plenum door and is used in place of a full door when hardware mounted to the plenum door does not require servicing.

5) All cabinets require power supplies adapted for 19" rack mounting. 17" rack panels can be converted to 19" by using extenders. Up to five power supplies can be mounted on a side frame.

6) When ordering stabilizer feet, H952-BA (pair) and/or kickplate 7406782, a short door or full door cannot be used in the cabinet front.

7) If fan assembly H952-CA is required, indicate the direction of desired air flow (up or down).

8) If using short door, make certain that the equipment for cabinet installation will not interfere with the door height.

9) The inner dimensions of the H950-AA frame on all (4) sides are 18-5/16. Consequently, it offers flexible panel rack expansion.

**Ordering Format** (Example)
When ordering H-950 hardware, use the following format:

| | | |
|---|---|---|
| 1. Frame 19" cabinet | H950-AA | 1 pc |
| Full door — RH | H950-CA | 1 pc |
| 5½ bezel cover panel | H950-P | 5 pcs |
| Fan assembly, air flow upwards | H952-CA | 1 pc |
| Caster set (4) | H952-EA | 1 set |
| Leveler set | H952-FA | 1 set |
| 2. Cabinet | ADD-ON CABINET | |
| add the following: | | |
| 5-¼" bezel cover panel | H950-P | 4 pcs |
| 10½" bezel cover panel | H950-Q | 2 pc |

| CABINET PARTS LIST | Parts No. |
|---|---|
| Frame 19″ wide, 25″ deep, 63″ mtg. panel includes cover filter and all mtg. hardware | H950-AA |
| Full door (RH) Front & Rear Door Mounting | H950-BA |
| Full door (LH) Front & Rear Door Mounting | H950-CA |
| Mounting panel door (plenum) RH rear mounting | H950-DA |
| Mounting panel door (plenum) LH rear mounting | H950-EA |
| Mounting panel door skin | H950-FA |
| Short door (covers 21″ mounting height) | H950-HA |
| Short door (covers 22¾″ mounting height) | H950-HB |
| Short door (covers 26¼″ mounting height) | H950-HC |
| Short door (covers 31½″ mounting height) | H950-HD |
| Short door (covers 36¾″ mounting height) | H950-HE |
| Short door (covers 42″ mounting height) | H950-HF |
| Short door (covers 47¼″ mounting height) | H950-HG |
| Short door (covers 52½″ mounting height) | H950-HH |
| Short door (covers 57¾″ mounting height) | H950-HJ |
| Short door (covers 63″ mounting height) | H950-HK |
| Frame panel (includes LOGO) | H950-LA |
| 5¼″ bezel cover panel (snap-on) | H950-P |
| 10½″ bezel cover panel (snap-on) | H950-Q |
| Filter (for fan assembly) | H950-SA |
| End panel (require 2 per cabinet) | H952-AA |
| Stabilizer feet (pair) | H952-BA |
| Fan assembly (specify direction of airflow) | H952-CA |
| Caster set (4) | H952-EA |
| Leveler set (4) | H952-FA |
| Filler strip — front & rear (joining two cabinets) | H952-GA |
| Kick plate | 7406782 |
| Kick plate (use with Add On cabinet) | 7406793 |

# ADD-ON OPTION CABINET

UNIVERSAL HARDWARE

The Add-on option cabinet uses the same H950-AA frame and parts as listed in the H950 and H952 parts list. It is designed for customers who want to add on to a basic cabinet system. It will house peripheral equipment for 19" panel rack mounting, especially those manufactured by DEC. Among the mounting options are 4K and 8K memory expansions, multiplexers, magnetic tape control transports, disk files, analog-to-digital converters, module racks, and power supplies. The cabinet is supplied without end panels, H952-AA, since the cabinet joins an existing basic system. The filler strip, H952-GA front and rear, are I-beams designed for compatibility between two or more cabinets.

The front part of the Add-on cabinet is equipped with a kick plate. The customer must remove the kick plate if a short door is to be used. The customer must specify what combination of bezels and/or short doors is needed to complete the front of cabinet. All parts are additional to quoted net price of the Add-on cabinet.

The Add-on cabinet includes all of the following:

| | Part No. |
|---|---|
| Frame — 19" wide, 63" mtg. panel height includes filter cover (less filter) | H950-AA |
| Mounting panel door skin | H950-FA |
| Mounting panel door (plenum) | H952-EA |
| Fan assembly — airflow upwards | H952-CA |
| Caster set (4) | H952-EA |
| Panel frame (includes LOGO) | H950-LA |
| Kick plate (to be used w/o stabilizer feet) | 7406793 |
| Filler strip front and rear (only used when joining cabinets) | H952-GA |
| Levelers | H952-FA |

**Ordering**
In order to efficiently assist the customer, we recommend that the customer specify the type of equipment intended for cabinets. Give the dimensions whenever possible to ensure exact cabinet configurations.

Before ordering hardware options for existing cabinets, make certain that they are compatible with the H950-AA standard frame, (overall height 71-7/16" from floor including casters, 19" wide frame, and 63" of vertical panel space). Module Marketing Services of Digital Equipment Corporation will assume responsibility only for parts ordered from the H950 and H952 Parts List.

**Color**
Basic color of cabinet hardware is black. Gray is used for end panels and the bezel of the cover panels.

Color changes will be accepted if customer's order is for 25 or more cabinets. Customer must supply color chips for colors desired.

**Shipping**
All shipments are FOB Maynard, Massachusetts. Specifications are subject to change without notice. Special packaging has been designed to ensure safe delivery with proper handling.

**Assembly**
The customer has the choice of cabinet configuration as listed in H950 and H952 Parts List. The customer must indicate whether the cabinet parts are to be shipped unassembled or completely assembled by Digital Equipment Corporation. See special consideration section.

**Discounts**
Same discounts that are applied to Modules. See Price List.

## COLOR CHANGES

Standard color of cabinets is black with gray end panels.

Customized painting will be accepted with a minimum order of 25 cabinets. Customer must supply a color chip for color desired. An additional charge of $20.00 will be added for each cabinet painted.

Order should be sent to Module Marketing Services.

No cabinet hardware will be accepted for credit or exchange without the prior written approval of DEC, plus proper return authorization number (RA#).

All shipments are FOB Maynard, Massachusetts, and prices do not include state or local taxes. Prices, discounts, and specifications are subject to change without notice.

Quantity Discounts (Module Discount applies)

| | |
|---|---|
| $ 5,000 — 3% | $ 100,000 — 18% |
| 10,000 — 5% | 250,000 — 21% |
| 20,000 — 10% | 500,000 — 22% |
| 50,000 — 15% | 1,000,000 — 25% |

## CABINET PRICE LIST MODULE PRODUCTS

| Catalog No. | Description | Price |
|---|---|---|
| H-920 | Module Drawer | $170.00 |
| H-921 | Front Panel | 10.00 |
| H-923 | Chassis Slides | 75.00 |
| H-925 | Moduie Drawer | 250.00 |
| H-950-AA | Frame | 152.00 |
| H-950-BA | Full Door (RH) | 31.00 |
| H-950-CA | Full Door (LH) | 31.00 |
| H-950-DA | Mtg Panel Door (RH) | 30.00 |
| H-950-EA | Mtg Panel Door (LH) | 30.00 |
| H-950-FA | Mtg Panel Door Skin | 21.00 |
| H-950-HA | Short Door (Covers 21" Mtg) | 57.00 |
| H-950-HB | Short Door (Covers 22¾" Mtg) | 57.00 |
| H-950-HC | Short Door (Covers 26¼" Mtg) | 57.00 |
| H-950-HD | Short Door (Covers 31½" Mtg) | 57.00 |
| H-950-HE | Short Door (Covers 36¾" Mtg) | 57.00 |
| H-950-HF | Short Door (Covers 42" Mtg) | 57.00 |
| H-950-HG | Short Door (Covers 47¼" Mtg) | 63.50 |
| H-950-HH | Short Door (Covers 52½" Mtg) | 63.50 |
| H-950-HJ | Short Door (Covers 57¾" Mtg) | 63.50 |
| H-950-HK | Short Door (Covers 63" Mtg) | 63.50 |
| H-950-LA | Frame Panel (includes Logo) | 16.00 |
| H-950-P | 5¼" Bezel Cover Panel | 10.00 |
| H-950-Q | 10½" Bezel Cover Panel | 12.00 |
| H-950-SA | Filter (for Fan Assembly) | 4.00 |
| H-952-AA | End Panel (2 per cab) | 39.00 |
| H-952-BA | Stabilizer feet (pair) | 25.50 |
| H-952-CA | Fan Assembly (specify air flow) | 54.50 |
| H-952-EA | Caster Set (4) | 14.50 |
| H-952-FA | Leveler Set (4) | 12.50 |
| H952-GA | Filler Strip F & R (joining two cabinets) | 44.00 |
| 7406782 | Kickplate | 4.00 |
| 7406793 | Kickplate (for use w/o Stabilizer Feet) | 5.50 |
| Add on Cabinet Unassembled | | 350.00 |
| Add on Cabinet Assembled | | 400.00 |

NOTE: Cabinets are shipped unassembled. For cabinet assembly a $50.00 charge will be added.

# WIRING ACCESSORIES
## 913, 914, 915, 917
## H820, H821, H825, H826



### 913 AND 915 PATCHCORDS

These patchcords provide slip-on connections for FLIP CHIP mounting panels and are available in color-coded lengths of 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, and 64 inches. All cords are shipped in quantities of 100 in handy polystyrene boxes. Type 913 patchcords are for 24 gauge wirewrap and use AMP Terminal Type #60530-1. Type 915 patchcords are for 30 gauge wirewrap and use AMP Terminal Type #85952-3.

### H820 AND H821 GRIP CLIPS FOR SHIP-ON PATCHCORDS

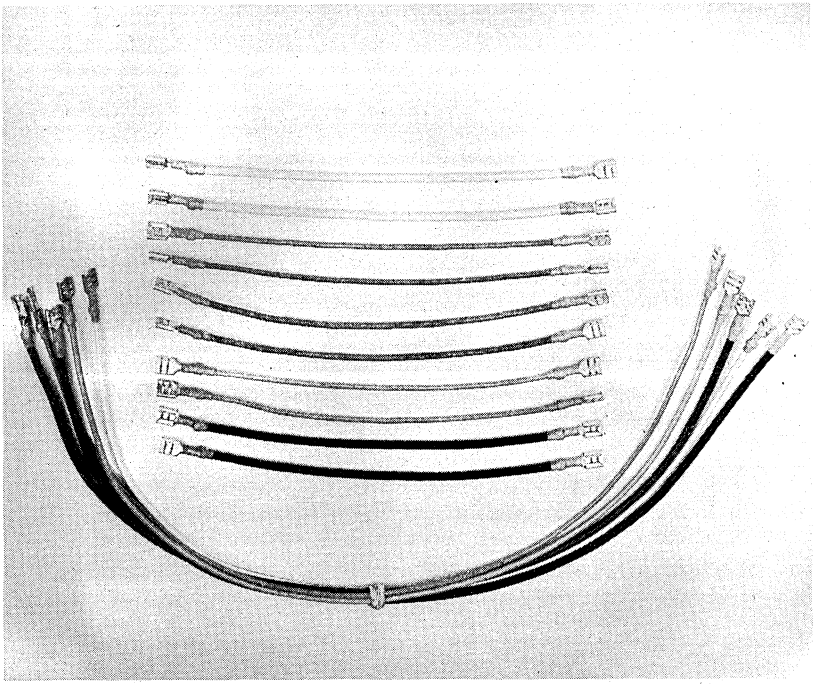
The type H820 and H821 GRIP CLIPS are identical to slip-on connectors used in respectively the 913 and 915 patchcords. These connectors are shipped in packages of 1000 and permit fabrication of patchcords to any desired length. H820 GRIP CLIPS will take size 24-20 awg. wire and may be purchased from AMP, Inc. as AMP part #60477-2. H821 GRIP CLIPS will take size 30-24 awg. wire and are AMP part #85952-3.

### H825 HAND CRIMPING TOOL

Type H825 hand crimping tool may be used to crimp the type H820 GRIP CLIP connectors. Use of this tool insures a good electrical connection. This tool may also be obtained from AMP, Inc. as AMP part #90084.

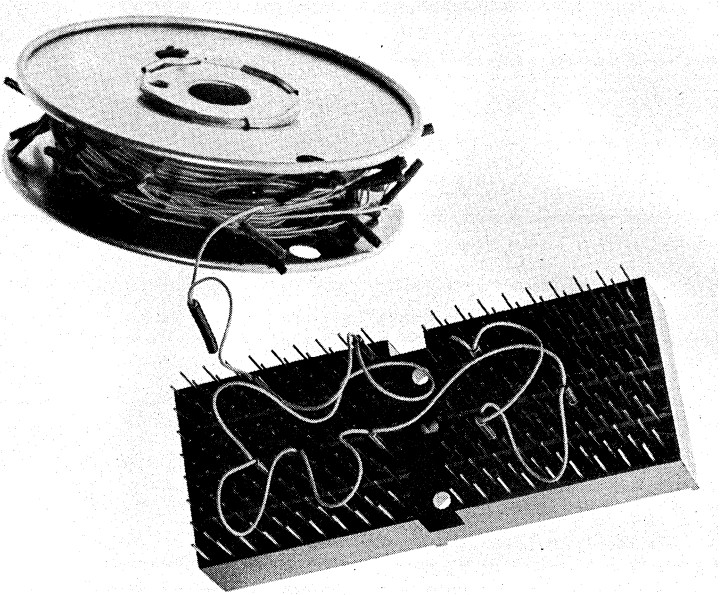
### H826 HAND CRIMPING TOOL

Type H826 hand crimping tool may be used to crimp the type H821 GRIP CLIP connectors. This tool is identical to AMP part #9019-1.



## 914 POWER JUMPERS

For interconnections between power supplies, mounting panels, and logic lab panels, these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers per package; 914-19 contains 10 jumpers per package.



## 917 DAISY CHAIN

Type 917 is a continuous length of unbroken #25 AWG stranded wire. 250 gold plated and insulated terminals are crimped at predetermined intervals on each reel. In conjunction with type H803 or type H807 connector blocks and M Series modules, hand patch wiring of prototype systems is easily and quickly accomplished. All that is required is a reel of type 917 Daisy Chain and wire cutters. These dependable push on connections are also easily removeable making this wiring technique ideal in cases where wiring and unwiring for changing systems needs is required. If ever a third lead is necessary a type 915 patchcord can be used if placed on the pin before the Type 917 termination. Two contact spacings available at 2½" or 5".

917 — 2.5 — blue
917 — 5 — white

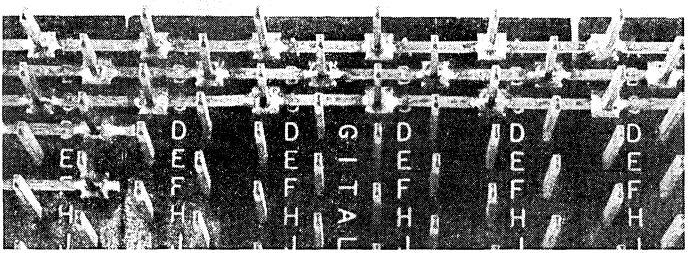
**Also available from:**
Berg Electronics
New Cumberland, Pa. 17070
Tel. (717) 938-6711

| | |
|---|---|
| 913 — | $ 18 pkg. of 100 |
| 914-7 — | $ 4 pkg. |
| 914-19 — | $ 4 pkg. |
| 915 — | $ 33 pkg. of 100 |
| H820 — | $ 48 pkg. of 1000 |
| H821 — | $ 75 pkg. of 1000 |
| H825 — | $146 |
| H826 — | $210 |

# WIRING ACCESSORIES

**932, 933, 934, 935, 936**
**H810, H811, H812, H813, H814**

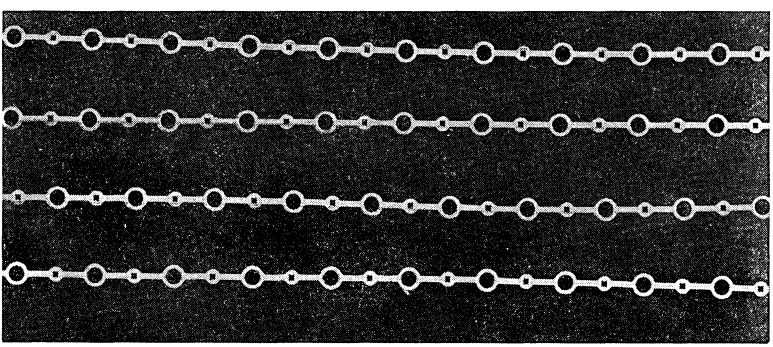




### 932 BUS STRIP

Simplifies wiring of register pulse busses, power, and grounds. Same as used in K943.

932 — $0.60



### 933 BUS STRIP

Simplifies wiring of power, ground and signal busses on mounting panels using H803 connectors.

933 — $1

### 934 WIRE-WRAPPING WIRE

1000 ft. roll of 24 gauge solid wire with tough, cut-resistant insulation. (Use Teflon insulated wire instead for soldering.)
For use with H800 connectors.

934 — $50

### 935 WIRE-WRAPPING WIRE

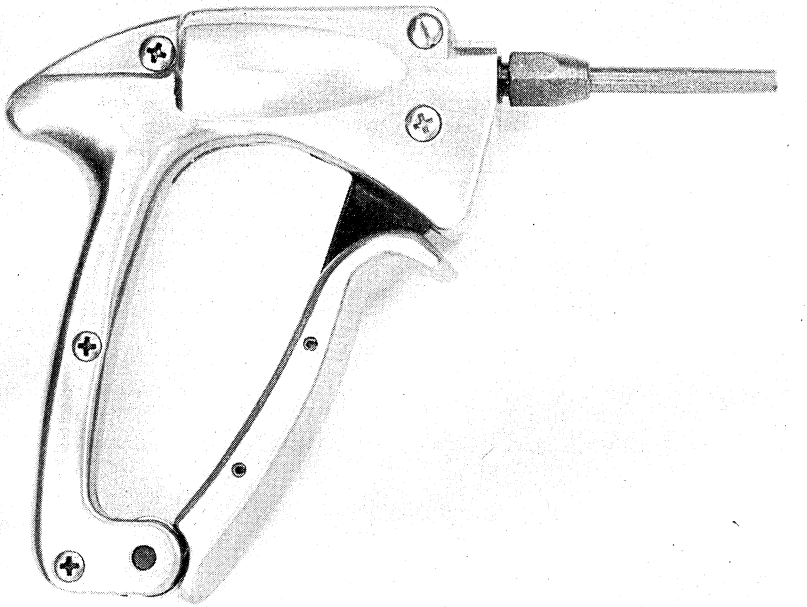
1000 foot roll or 30 gauge insulated solid wire for use with H803 connectors.

935 — $60

### 936 19 CONDUCTOR RIBBON CABLE

Use on W Series connector modules or split into 9-conductor cables for use with K580, K681, K683, etc.

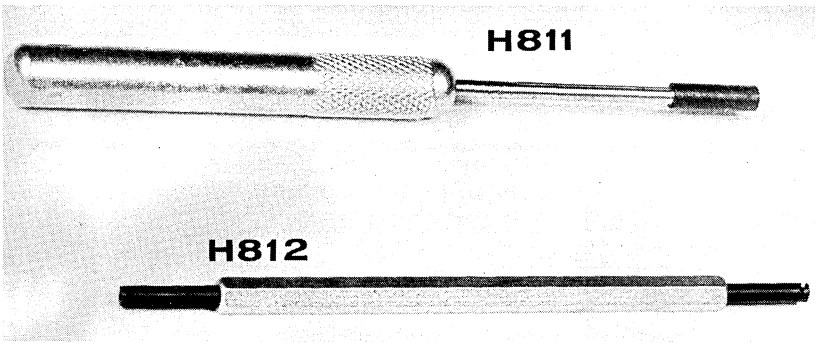
936 — $0.60



### H810 PISTOL GRIP HAND WIRE WRAPPING TOOL

The type H810 Wire Wrapping Tool is designed for wrapping #24 or #30 solid wire on Digital-type connector pins. The H810 Kit includes the proper sleeves and bits. It is recommended that five turns of bare wire be wrapped on these pins. This tool may also be purchased from Gardner-Denver Co. (Gardner-Denver part No. 14H-1C) with No. 26263 bit and No. 18840 sleeve for wrapping #24 wire. Specify bit #504221 and sleeve #500350 for wrapping #30 wire. When ordering from Digital specify the sleeve and bit size desired for #24 and #30 wire.

H810(24) — $ 99
H810A — $ 99
H810B — $150




The Type H811 Hand Wrapping tool is useful for service or repair applications. It is designed for wrapping #24 solid wire on DEC Type H800-W connector pins. This tool may also be purchased from Gardner-Denver Co. as Gardner-Denver Part #A20557-12.

Wire wrapped connections may be removed with the Type H812 Hand Unwrapping tool. This tool may also be purchased from Gardner-Denver Co. as Gardner-Denver Part #500130.

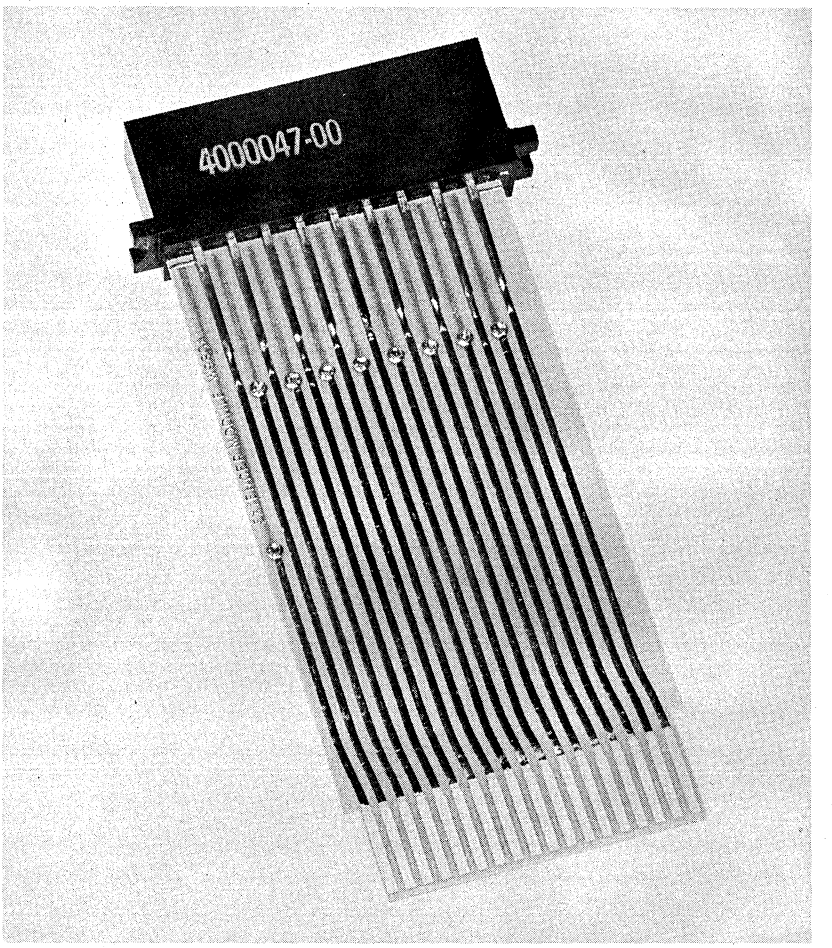
The H811A and H12A are equivalent to the H811 and the H812 except that the A versions are designed for #30 wire. Both tools may be purchased from Gardner-Denver directly under the following part numbers: H811A A-20557-29; H812A 505 244-475. The H813 is a #24 bit; H813A, a #30 bit. The H814 is a #24 sleeve; H814A, a #30 sleeve.

None of the Wire Wrapping Tools will be accepted for credit under any circumstances.

| | |
|---|---|
| H811(24) | $21.50 |
| H811A(30) | $21.50 |
| H812(24) | $10.50 |
| H812A(30) | $10.50 |
| H813(24) | $30 |
| H813A(30) | $30 |
| H814(24) | $21 |
| H814A(30) | $21 |

# MODULE EXTENDER
## W980,

UNIVERSAL HARDWARE



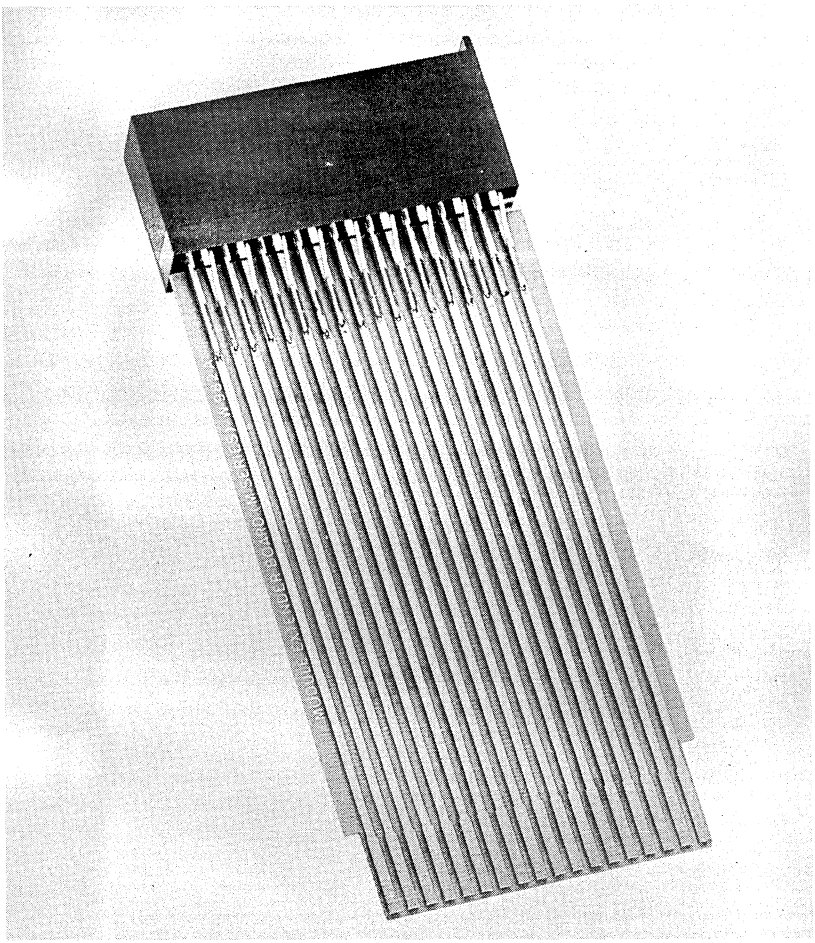

The W980 Module Extender allows access to the module circuits without breaking connections between the module and mounting panel wiring.

For double size flip-chip modules use two W980 extenders side by side. The W980 is for use with A, K and W Series 18 pin modules.

W980 — $14

# MODULE EXTENDER
W982,

UNIVERSAL HARDWARE



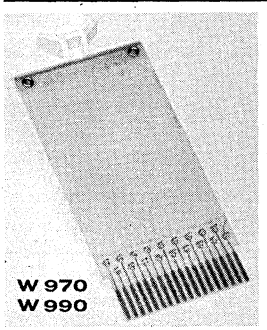
The W982 serves a function similar to the W980 except it contains 36 pins for use with M series modules. The W982 can be used with all modules in this catalog. A, K, and W series modules will make contact with only 2 side pins. A2, B2, etc.

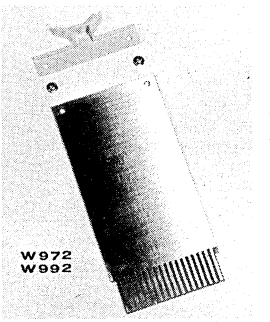
For double size M Series modules use two W982 extenders side by side.

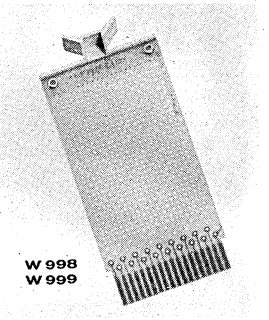
W982 — $18

# BLANK MODULES
## W970-W975, W990-W999

**UNIVERSAL HARDWARE**



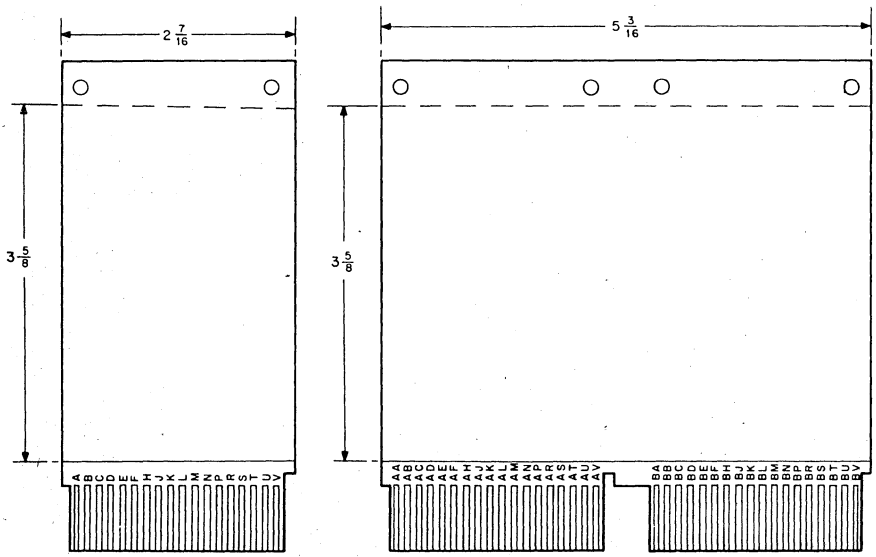

These 10 blank modules offer convenient means of integrating special circuits and even small mechanical components into a FLIP CHIP system, without loss of modularity. Both single- and double-size boards are supplied with contact area etched and gold plated. The W990 Series modules provide connector pins on only one module side for use with H800 connector blocks. W970 series modules have etched contacts on both sides of the module for use with double density connectors Type H803, and low density Type H808.

| Type | Pins | Description | Handle | Price |
|---|---|---|---|---|
| W990 | 18 | Bare board, split-lug terminals | attached | $ 2.50 |
| W991 | 36 | Bare board, split-lug terminals | attached | $ 5.00 |
| W992 | 18 | Copper clad, to be etched by user | separate | $ 2.00 |
| W993 | 36 | Copper clad, to be etched by user | separate | $ 4.00 |
| W998 | 18 | Perforated, 0.052" holes, 18 with etched lands. The holes are on 0.1" centers, both horizontally and vertically. | attached | $ 4.50 |
| W999 | 36 | Perforated, 0.052" holes, 36 with etched lands. The holes are on 0.1" centers, both horizontally and vertically. | attached | $ 9.00 |
| W970 | 36 | Bare board, no split lugs, similar to W990, contact both sides | attached | $ 4.00 |
| W971 | 72 | Bare board, no split lugs, similar to W991, contact both sides | attached | $ 8.00 |
| W972 | 36 | Copper clad, similar to W992 | separate | $ 4.00 |
| W973 | 72 | Copper clad, similar to W993 | separate | $ 6.00 |
| W974 | 36 | same as W998, contact both sides | attached | $ 9.00 |
| W975 | 72 | same as W999, contact both sides | attached | $18.00 |

Old boards with .067" holes on .2" centers are no longer available.

# BLANK COPPER CLAD MODULES
## W992, W993, W972, W973

**UNIVERSAL HARDWARE**




W992 W993

Type W992 and W993 are single side copper clad boards. The diagrams above indicate the copper clad area that is usable for etching purposes. The identifying numbers are etched from the clad using a minimum of etchable area. Type W972 and W973 are equivalent to the above types but have copper clad on both sides.

W972 — $4
W973 — $6
W992 — $2
W993 — $4

# ORDERING INFORMATION FOR PREASSEMBLED CABLE

**UNIVERSAL HARDWARE**

Standard lengths for preassembled cable are: 3, 5, 7, 10, 15 and 25 feet.

Cable price per foot is as follows:

| | |
|---|---|
| 19 conductor Ribbon cable | $0.60 |
| 9 conductor Flat Coaxial cable | $1.00 |
| 19 conductor 1¼" Mylar cable (BC08 only) | $0.75 |

Standard charges for connection of cable to each connector is as follows:

| | |
|---|---|
| Ribbon | $ 9.00 per connector side |
| Coaxial | $18.00 per connector side |
| Mylar | $ 3.00 per connector side |

STANDARD PREASSEMBLED CABLES

RIBBON

| Type | CONNECTORS | Basic Price |
|---|---|---|
| BC02F-XX | W018-W023 | 31.00 |
| BC02L-XX | W021-W021 | 26.00 |
| BC02M-XX | W021-W022 | 27.00 |
| BC02P-XX | W022-W022 | 28.00 |
| BC02S-XX | W023-W023 | 26.00 |
| BC02W-XX | W028-W028 | 28.00 |

COAXIAL

| Type | CONNECTORS | Basic Price |
|---|---|---|
| BC03C-XX | W021-W021 | 44.00 |
| BC03D-XX | W021-W022 | 45.00 |

To the above prices, add price of cable:

Example: BC02L-7 $30.20

| | |
|---|---|
| 1—BC02L-XX | $26.00 |
| 7 feet ribbon cable @ $0.60/ft. | 4.20 |
| | $30.20 |

Standard preassembled cables are available in lengths of 3, 5, 7, 10, 15 or 25 feet. The last figure in the part number indicates the cable length. For example, BC08-A-10 is a 1¼" Mylar Cable 10 feet long with an M903 connector at each end.

**STANDARD M SERIES CABLES**

| 1¼" Mylar Cable with M903-M903 Connectors | |
|---|---|
| BC08-A-1 | $37.50 |
| BC08-A-2 | 39.00 |
| BC08-A-3 | 40.50 |
| BC08-A-4 | 42.00 |
| BC08-A-5 | 43.50 |
| BC08-A-6 | 45.00 |
| BC08-A-7 | 46.50 |
| BC08-A-8 | 48.00 |
| BC08-A-9 | 49.50 |
| BC08-A-10 | 51.00 |
| BC08-A-15 | 58.50 |
| BC08-A-25 | 73.50 |

| Flat Coax Cable with M904-M904 Connectors | |
|---|---|
| BC08-B-1 | $ 82.00 |
| BC08-B-2 | 84.00 |
| BC08-B-3 | 86.00 |
| BC08-B-4 | 88.00 |
| BC08-B-5 | 90.00 |
| BC08-B-6 | 92.00 |
| BC08-B-7 | 94.00 |
| BC08-B-8 | 96.00 |
| BC08-B-9 | 98.00 |
| BC08-B-10 | 100.00 |
| BC08-B-15 | 110.00 |
| BC08-B-25 | 130.00 |

| 1¼" Mylar Cable with M903 & 2 W031 Connectors | |
|---|---|
| BC08-C-1 | $ 34.00 |
| BC08-C-2 | 35.50 |
| BC08-C-3 | 37.00 |
| BC08-C-4 | 38.50 |
| BC08-C-5 | 40.00 |
| BC08-C-6 | 41.50 |
| BC08-C-7 | 43.00 |
| BC08-C-8 | 44.50 |
| BC08-C-9 | 46.00 |
| BC08-C-10 | 47.50 |
| BC08-C-15 | 55.00 |
| BC08-C-25 | 70.00 |

| Flat Coax Cable with M904 & 2 W011 Connectors | |
|---|---|
| BC08-D-1 | $ 77.00 |
| BC08-D-2 | 79.00 |
| BC08-D-3 | 81.00 |
| BC08-D-4 | 83.00 |
| BC08-D-5 | 85.00 |
| BC08-D-6 | 87.00 |
| BC08-D-7 | 89.00 |
| BC08-D-8 | 91.00 |
| BC08-D-9 | 93.00 |
| BC08-D-10 | 95.00 |
| BC08-D-15 | 105.00 |
| BC08-D-25 | 125.00 |

# CABLE CONNECTORS FOR INDICATOR AMPLIFIERS

**W018, W023**

**W SERIES**

The W018 and W023 provide 18 line ribbon cable connections to FLIP CHIP mounting panels. In the W018 connection to each pin is through a series low leakage silicon diode. The W023 provides unbroken signal lines from the cable to the connector pin.

When these cables are used with 4917 or 4918 indicators, the W018 must be located at the FLIP CHIP panel and the W023 inserted in the indicator socket connector. Cables may be ordered with connector modules on both ends or on one end only. Cable lengths may be specified in increments of 1 inch.

For ordering information, see W021, W022, and W028 on next page.

Care should be taken when using the W023 for other purposes, since the Power Pins (A, B) are unprotected.

| Type | Price without Cable |
|---|---|
| W018 | $9.00 |
| W023 | $4.00 |

# CABLE CONNECTORS FOR LEVELS AND PULSES

**TYPES W021, W022, W028**

**W SERIES**

The W021, W022, and W028 provide cable connections to the FLIP CHIP mounting panel. The cable is a 19-conductor ribbon with nine signal leads and ten shields. The signal leads are connected to pins D, E, H, K, M, P, S, T and V. The shields are internally connected together and to pins C, F, J, L, N, R, and U.

In the W021, the signal leads are connected directly to the signal pins. In the W028, jumpers are available for series or shunt terminators. The Type W022 has a 100-ohm shunt terminator from each signal wire to the shield.

W021 — $4.00
W022 — $5.00
W028 — $5.00

# DIGITAL WIRE WRAP SERVICES

The electronics industry has long been aware of the many advantages of wire wrapping over soldering for interconnecting electronic circuits. Soldering introduces numerous human errors and presents problems of cold solder joints, flux removal and overheating sensitive components. Automatic, computer-controlled wire wrapping, however, not only eliminates the problems associated with soldering but adds many technical and economic benefits unattainable with soldering. Automatic wire wrap provides extremely high reliability, high production rates, elimination of human error, long-life connections, simple mechanical inspection techniques, high density wiring, rework ability, reduced labor and reduced inspection time.

Digital Equipment Corporation has developed an extensive high-production wire wrapping capability and now offers to its customers the significant cost savings of automatic wire wrapping. Digital can provide a full wire wrap service and our "Smooth-Flow" processing insures maximum control at each step in the process.

Digital automatically verifies the correctness of the wiring on each panel with its computer-controlled Automatic Wire Test equipment. This verification is a standard part of Digital's wire wrap service and is provided at no charge. The only restriction is that the size of the panel be limited to four connector blocks high by ten connector blocks wide. No price reduction is given for elimination of the verification service.

Before a wire wrap order can go into production, Digital needs from the customer a deck of punched cards for use as input to the wire list program. If the customer wishes, Digital can provide a keypunching service to prepare the punched cards. For this service, Digital needs a customer wire listing prepared on Digital Form DR22. Either the punched cards or Form DR22 must also be accompanied by a purchase order specifying which mounting panels are being purchased. In addition, if any special bussing is needed, a copy of the updated bussing diagram must also accompany the purchase order. It is extremely important that a complete wire listing, either punched cards or Form DR22 mounting panel specification, and complete bussing information be received with each order. Pricing of a wire wrap order cannot be completed until the source deck has been processed and buss print received. These are needed to determine wire count and number of points to be bussed.

**Special Services**

Digital keypunching service is provided at the rate of $0.10 per card. This service includes customer source input verification.

If the customer wishes to have a magnetic tape of the listing, DEC will prepare a tape in card image for $35 per reel. The customer will receive one copy each of the Name Sort and Pin Sort lists. Additional copies of these lists are available to the customer for $10 each upon his written request.

Digital will perform special bussing where required. The rate for this is $0.10 per point, plus the price of the buss strip (932, $0.60 each; 933, $1 each). If errors are found in a customer-supplied source deck or wire list, the customer will be contacted to make the necessary corrections. There is a flat service fee of $50, non-discountable, for detecting customer-source errors.

**Delivery**

The normal delivery time for wire wrap panels is four to six weeks after receipt of the purchase order, accurate source inputs (card or wire list), and updated bussing diagram if special bussing is required. In cases where extensive special bussing is required additional time should be allowed for delivery (approximately two weeks). If customer-source errors are detected, allow at least one additional week.

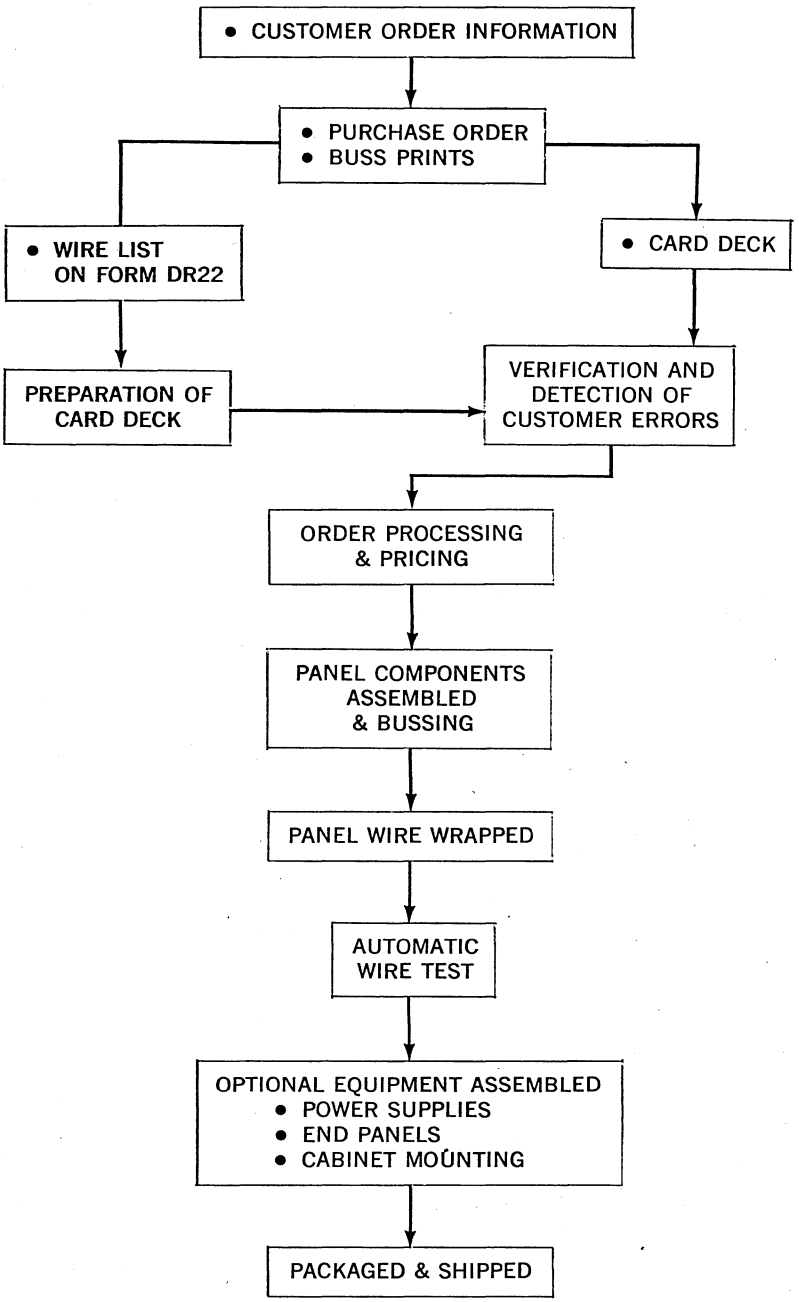
On repeat orders for the same panels and wiring configuration, normal delivery time is often reduced to almost half that of initial processing time.

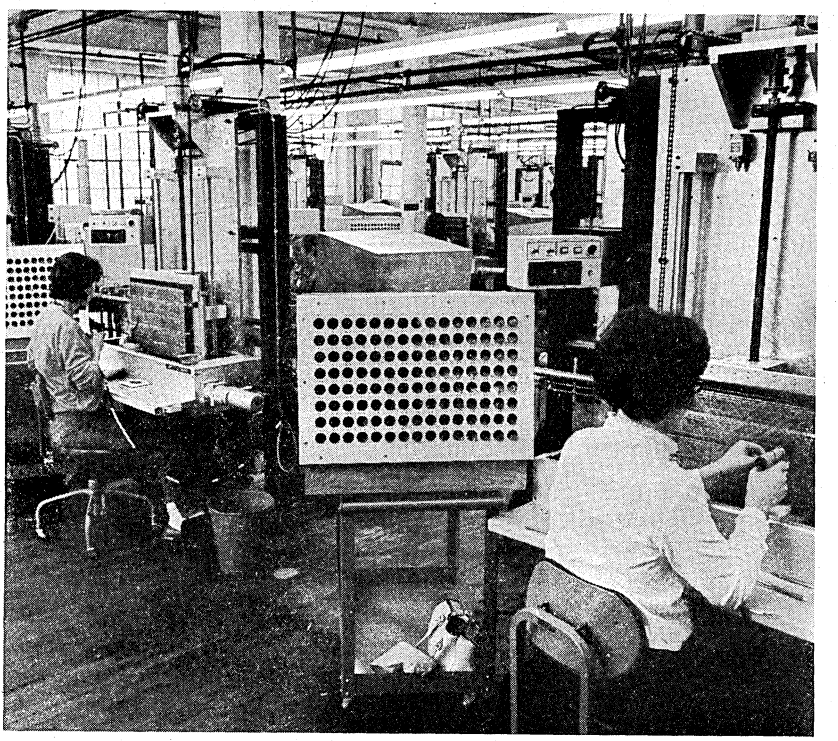
## PRICING

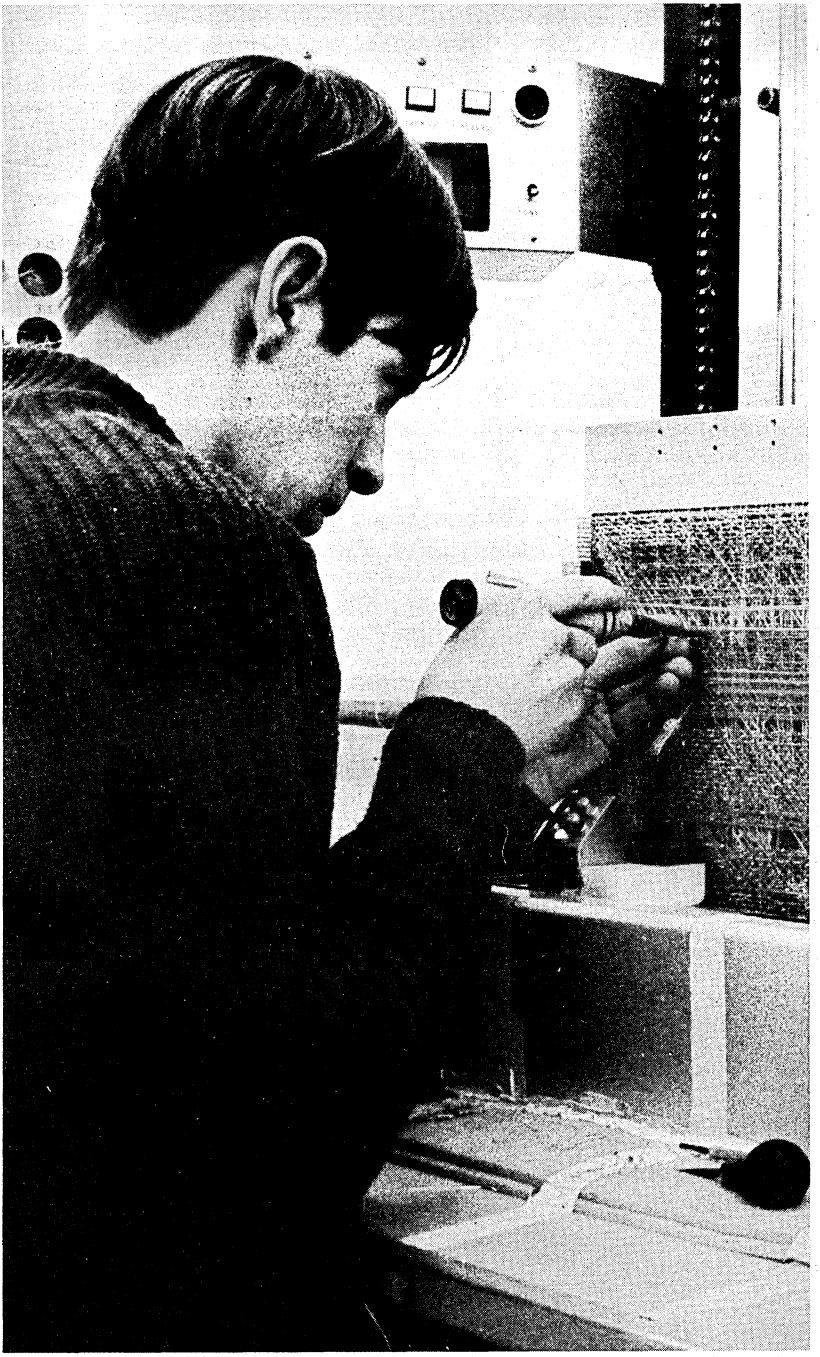
| | |
|---|---|
| 24 ga Wire: | |
| Set-up Charges (do not include price of panels) | |
| One-time charge for up to four panels | $320.00* |
| Each additional panel | 25.00 |
| Cost per Wire | .25 |
| 30 ga Wire: | |
| Set-up Charges (do not include price of panels) | |
| One-time charge for up to two panels | 200.00* |
| Each additional panel | 50.00 |
| Cost per Wire | .30 |
| Digital Cardpunching Service, per card | .10 |
| Customer-error Detection | 50.00* |
| Magnetic Tape of Wire List | 35.00* |
| Additional Copies of Name Sort and Pin Sort List, each | 10.00 |
| Special Bussing, per point | .10 |
| 933 Buss Strip | 1.00 |
| 932 Buss Strip | .60 |
| Automatic Wiring Verification | No Charge |

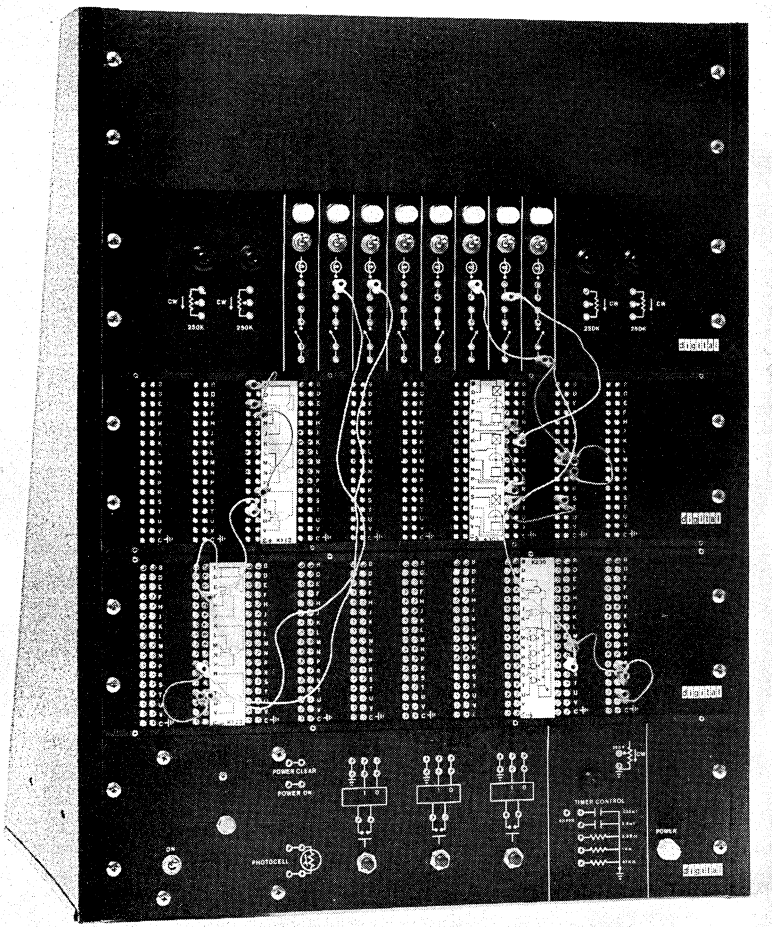
*One time charges are not discountable

The following chart illustrates Digital's wire wrap order processing.








250K
250K
POWER CLEAR
POWER ON
PHOTOCELL
TIMER CONTROL
POWER

# K-SERIES
# LOGIC LAB

## INTRODUCTION

The K Series Logic Laboratory is designed for use with K Series Modules. It is a device for building prototype systems for experimentation and proof of logic design as well as an effective tool for learning solid state control logic.

It is excellent for training users in digital logic techniques by enabling an individual to construct logical networks, with a "hands on approach" to learning control systems for Industrial Applications.

The K Series Logic Lab is a completely self contained system consisting of a power supply, photo cell, pulse generator, switch controls, indicators, mounting hardware and a recommended basic complement of logic modules necessary to construct a working system. The system is expandable and can accommodate additional K901 patchboard panels for mounting additional logic modules.

## EDUCATION AND TRAINING

As a training device the K Series Logic Lab offers the engineer, technician, and user a step by step approach to building an understanding of various digital logic functions, such as, AND, OR and the operations of NAND and NOR etc. The user has the option of using NEMA or MIL spec symbology when making logic connections. Symbology cards on basic logic modules for use with the K901 patchboard panel are printed with NEMA on one side and MIL SPEC 806 on the reverse side.

## BREADBOARDING AND TESTING

The logic laboratory power supply is capable of supplying 5V-DC for about 100 modules. There is no restriction on the size of a system which can be implemented, since additional patchboard panels can be ordered and "K" Logic Laboratories interconnected directly.

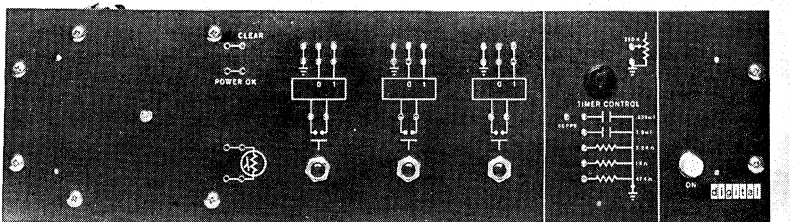
There is no substitute for actually building the system and verifying the logic.

Some common uses of the Logic Laboratory are listed below. Many of these are described in detail in the Control Handbook and part III in the 1969 Positive Edition Logic Handbook.

| | |
|---|---|
| Timer Sequencers | Serial Adder |
| Shifter Sequencers | Stepping Motors Control |
| Parallel Counters | Pulse Generator |
| Pulse Rate Multiplier | Annunciator |

# CONTROL PANEL — POWER SUPPLY
## K900

**K SERIES**




The K900 is a combination power supply and input control panel. The input devices include a photocell, three push button pulsers and timing components for a K303 clock mounted in a K901 panel. Clock timing components are provided for frequency steps in ranges of 2Hz to 60Hz and 200Hz to 6K Hz. Wiring diagrams for properly connecting the clock are shown in the logic and control handbooks (reference K303). The power supply can drive approximately ten type K901 panels of K series flip chip™ logic. Pulsers consist of a K501 schmitt trigger with a K581 switch filter. Power is supplied by K731, K743 and K732 power supply modules.

### Electrical Characteristics

Input voltage: Power supply: 115V 50-60 cps
Output voltage: +5 VDC ±10%
Output current: 3 amp

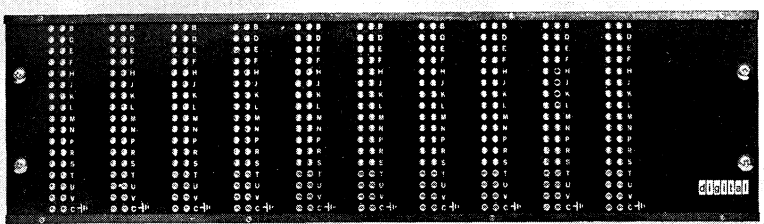
### Mechanical Characteristics

Panel width: 19″
Panel height: 5 3/16″
Depth: 12″
Finish: black
Power Unit connection: 18/3 AC power cord
Power Output connection: Hayman Tab terminals which fit AMP "Faston" receptacle series 250, part 41774 or Type 914 Power Jumpers.

**K900 — $185**

# PATCH BOARD PANEL
K901, 911

**K SERIES**



## K901 PATCHCORD MOUNTING PANEL

This panel provides up to ten FLIP CHIP modules with power and patch connections. Space between patching sockets allows insertion of logic diagrams. Logic diagrams are printed on all FLIP CHIP module data sheets. More permanent plastic diagrams are available for those modules listed.

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5 3/16 in.
DEPTH: 6½ in. with FLIP CHIP modules inserted

FINISH: Black
POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

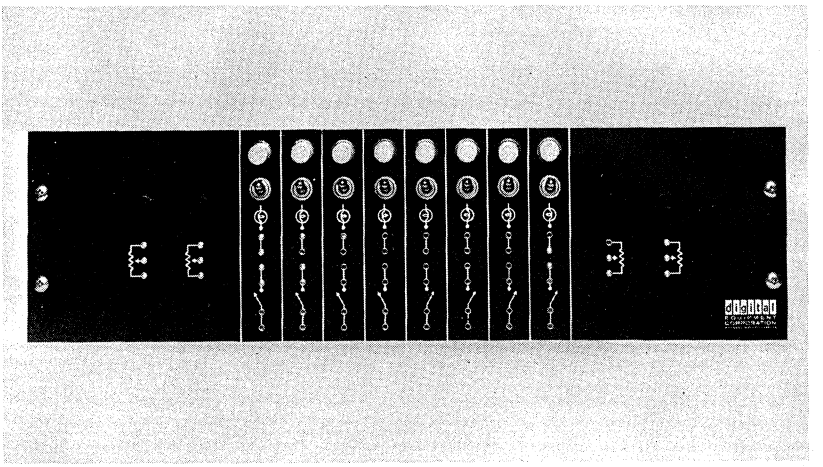
## 911 PATCHCORDS

DEC Type 911 Banana-Jack Patchcords are supplied in color-coded lengths of 2 in. (brown), 4 in. (red), 8 in. (orange), 16 in. (yellow), 32 in. (green), and 64 in. (blue). Patchcords may be stacked to permit multiple connections at any circuit point on the graphic panels of the DEC K901 Mounting Panel. The cords are supplied in snap-lid plastic boxes of ten for handy storage.

H901 — $125
911 — $9/pkg. of 10

# INDICATOR SWITCH PANEL
## K902

**K SERIES**



The H902 Panel provides facilities for control and observation of the Logic Laboratory. It contains eight indicator lights and a lamp driver module, eight toggle switches and four potentiometers. Connections to these devices are made with Type 911 Stacking Banana-Jack Patchcords.

INDICATORS: Indicators inputs accepts signals of +5V and ground. An open circuit input will light the indicator. If the input is returned to ground, the indicator will not light. The load is 1 ma.

TOGGLE SWITCHES: The toggle switches are single pole, single throw with a logic diagram to show the open and closed positions.

POTENTIOMETERS: The potentiometers are 250,000 ohms. They may be used to control the frequency of delay one-shots or clock circuits in the K901 Mounting Panel.

### MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5 3/16 in.
DEPTH: 6 1/2 in.

FINISH: Black
POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

K902 — $145

# MISCELLANEOUS ACCESSORIES
4913, 914

HARDWARE

## 4913 MOUNTING RACK

The 4913 Mounting Rack provides support for a and up to four K901 Patchcord Mounting Panels, for a total of up to 40 FLIP CHIP modules ready to be patched together for experiments. It may also be used to mount general purpose mounting panels such as the K943. The power supply must be mounted at the bottom for stability.

Height: 26¼ in.

Threads for mounting panels: 10-32

## 914 POWER JUMPERS

For interconnections between power supplies, mounting panels, and logic lab panels, these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers; 914-19 contains 5.

| | |
|---|---|
| 4913K | $25 |
| 914-7 | $ 4 |
| 914-19 | $ 4 |

## BASIC EQUIPMENT LISTS

### BASIC LOGIC LABORATORY

| | | |
|---|---|---|
| 1-K901 | Patchboard panel | 125.00 |
| 1-K902 | Indicator Switch Panel (complete with K683 module) | 145.00 |
| 1-K900 | Power Supply and Control Panel (complete with Power modules) | 185.00 |
| 1 pair — 4913 | Mounting Rack | 25.00 |

## RECOMMENDED LOGIC MODULES AND PATCHCORDS FOR USE WITH THE LOGIC LABORATORY

| | | UNIT PRICE | TOTAL PRICE |
|---|---|---|---|
| 4-K003 | Expander | 5.00 | 20.00 |
| 2-K012 | Expander | 8.00 | 16.00 |
| 3-K113 | Gate | 11.00 | 33.00 |
| 3-K-123 | Gate | 12.00 | 36.00 |
| 2-K134 | Inverter | 13.00 | 26.00 |
| 1-K161 | Decoder | 25.00 | 25.00 |
| 1-K174 | Comparator | 24.00 | 24.00 |
| 1-K184 | Rate Multiplier | 25.00 | 25.00 |
| 2-K202 | Flip-flop | 27.00 | 54.00 |
| 1-K206 | Flip-flop | 20.00 | 20.00 |
| 2-K210 | Counter | 27.00 | 54.00 |
| 1-K220 | Up-down Counter | 55.00 | 55.00 |
| 1-K230 | Shift Register | 40.00 | 40.00 |
| 1-K303 | Timer | 27.00 | 27.00 |
| 1-K323 | One shot delay | 35.00 | 35.00 |
| 1-K376* | Timer Control (0.1-3.0 sec) | 15.00 | 15.00 |
| 1-K378* | Timer Control (1.0-30 sec) | 15.00 | 15.00 |
| 1-K373* | Timer Control (20 Hz-600 Hz clock) | 11.00 | 11.00 |
| 1-K522 | Sensor Converter | 25.00 | 25.00 |
| | | | |
| 4 pks. of 10 patchcords (911-2″) | | 9.00 | 36.00 |
| 5 pks. of 10 patchcords (911-4″) | | 9.00 | 45.00 |
| 2 pks. of 10 patchcords (911-16″) | | 9.00 | 9.00 |
| 1 pkg. of 10 patchcords (911-16″) | | 9.00 | 9.00 |
| 26 symbology cards | | .25 ea. | 6.50 |

Complete K-Series logic lab with workbook and modules listed — H510 $995.00

Asterisk* denotes symbology cards unavailable. Symbology cards for use with K901 patchboard panel, .25 ea., minimum purchase of $5.00 applies.

## IF ADDITIONAL K901 PATCHBOARDS ARE ORDERED:

| | | |
|---|---|---|
| 1-911-4″ | pkg. of 10 patchcords | 9.00 |
| 1-911-8″ | pkg. of 10 patchcords | 9.00 |
| 1-911-16″ | pkg. of 10 patchcords | 9.00 |
| 1-911-32″ | pkg. of 10 patchcords | 9.00 |

## K-SERIES INTERFACE MODULES

Recommended logic modules for input/output functions.

**AC Input/Output**

| | | |
|---|---|---|
| 1-K578 | 120 VAC Input converter | 80.00 |
| 1-K614 | 120 VAC Isolated AC switch | 88.00 |

**DC Input/Output**

| | | |
|---|---|---|
| 1-K580 | Dry Contact Filter | 28.00 |

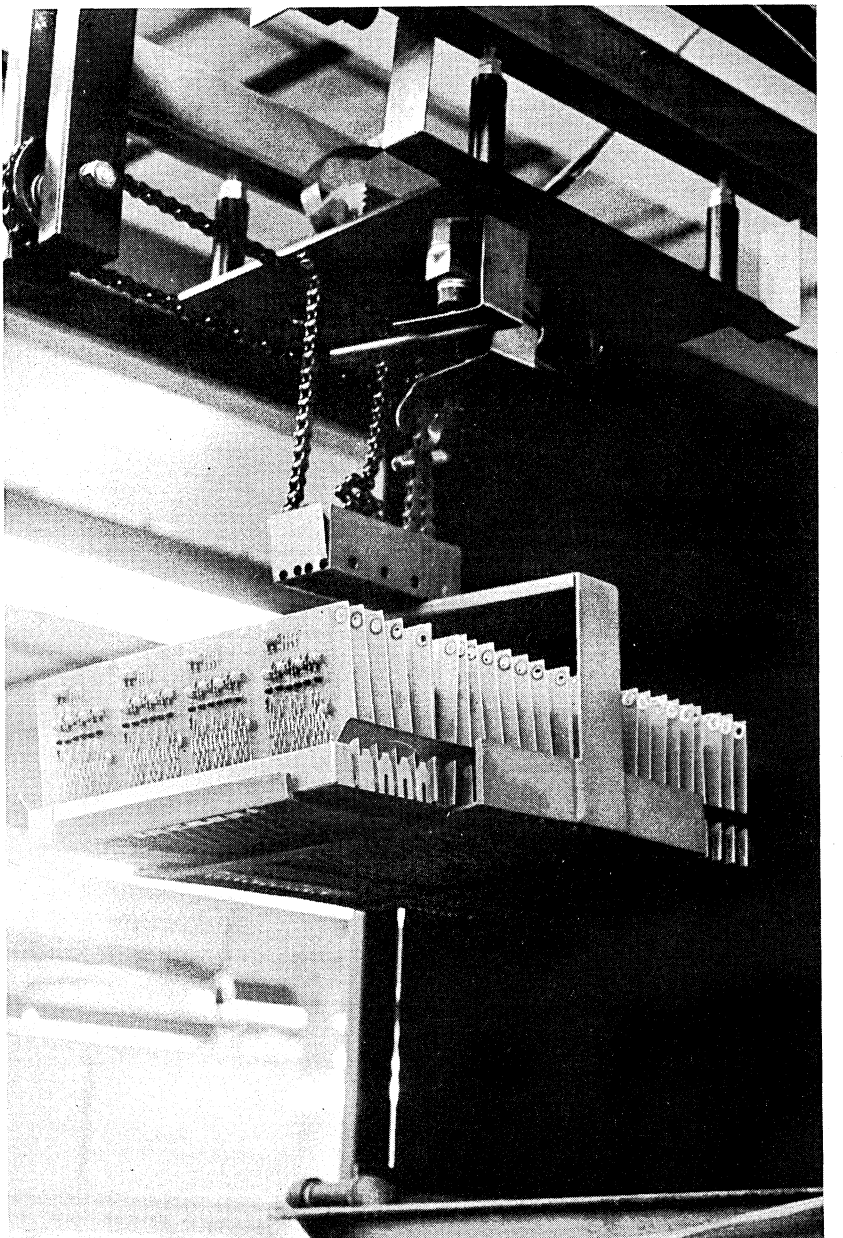
Listed below are a number of DC output drivers that may be used:

| | | |
|---|---|---|
| 1-K644 | DC output Driver | 66.00 |
| | or | |
| 1-K656 | DC output Driver | 80.00 |
| | or | |
| 1-K658 | DC Output Driver | 128.00 |

| | |
|---|---|
| Each additional K series workbook | 5.00 |

Note: only 3 out of 4 circuits are available when using above 3 modules with the K901 mounting panel.

Reference logic or control handbook for additional module information and selection.



After all the components have been attached to the board, the module is degreased to remove contaminants in preparation for flow soldering.

# PART III
# APPLICATIONS

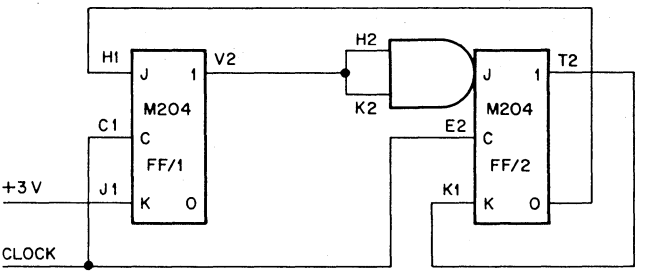
# COUNTER APPLICATIONS
## M204



The arrangement of the J-K flip-flops on the M204 was designed to allow its use as a general purpose clocked counter with a minimum of external gating. This note describes configurations up to modulus 10 (binary coded decimal). In this range only modulus 7 requires additional hardware. The basic design principle used in these counters is to detect the present state of the counter and decide whether or not to complement the flip-flops on the next clock pulse.

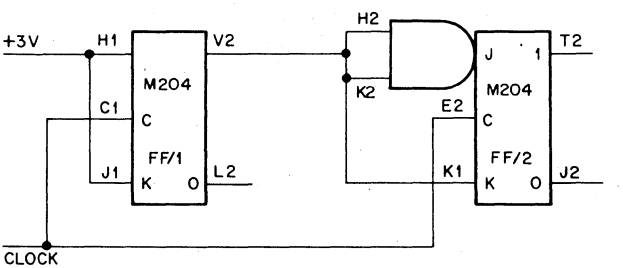
Other techniques exist for making counters of this type making use of pulse amplifiers etc., but these usually represent a significant increase in price.

It must be noted that the line defined as "Clock" requires a positive pulse which is the logical inversion of the standard pulse. One gate of an M117 can be used to perform this inversion. Since each clock input presents two unit loads to the source, more than 5 stages of counting requires the use of one gate of an M627. (Refer to the "Timing Considerations" section of the Logic Handbook.)



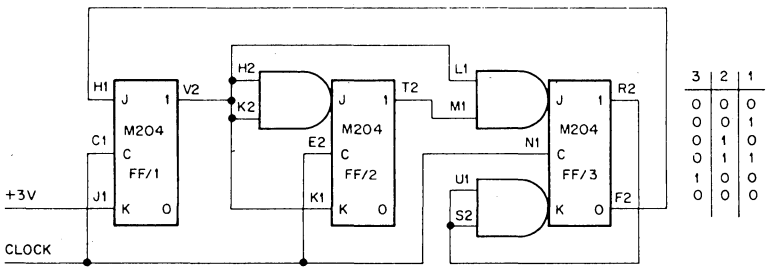

| 2 | 1 |
|---|---|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 0 | 0 |

MODULUS 3



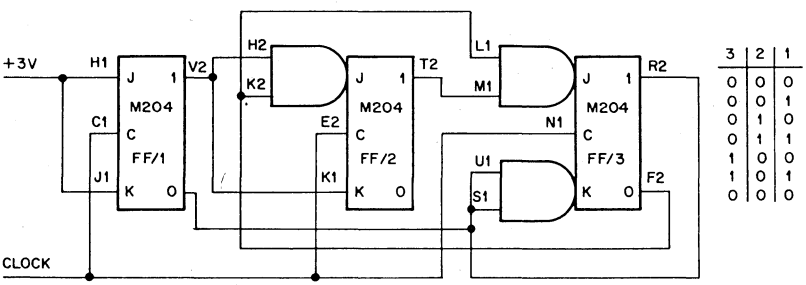

| 2 | 1 |
|---|---|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |
| 0 | 0 |

MODULUS 4



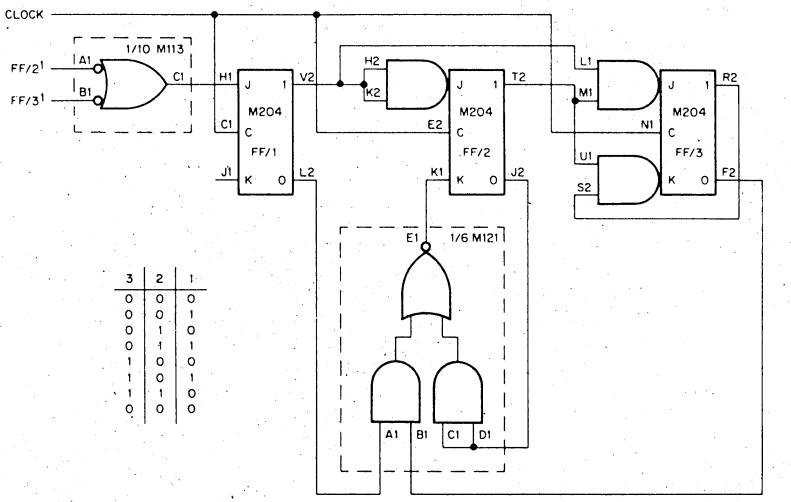

| 3 | 2 | 1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 0 | 0 |

MODULUS 5



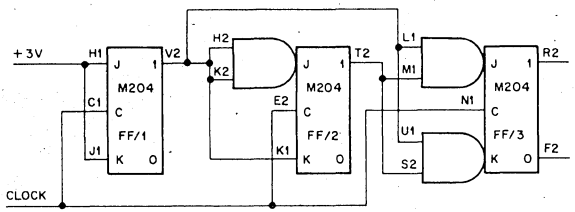

| 3 | 2 | 1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 0 | 0 |

MODULUS 6



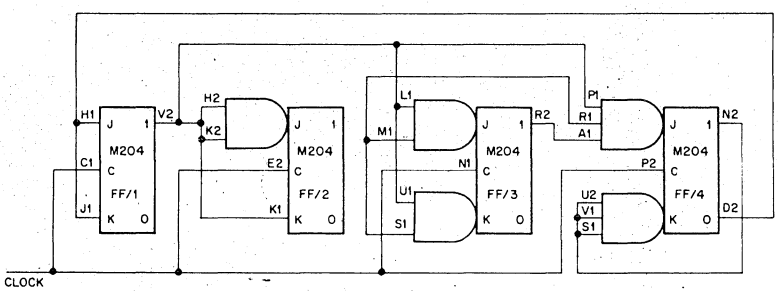

MODULUS 7

The modulus 7 counter requires external gating and cannot be implemented with the M204 alone.



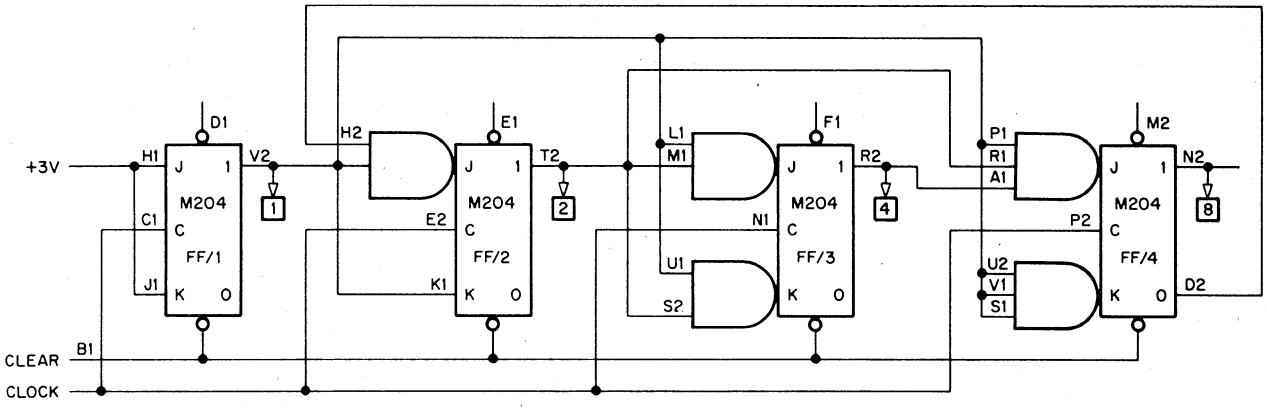

| 3 | 2 | 1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 1 |
| - | - | - |
| 0 | 0 | 0 |

MODULUS 8




MODULUS 9

| 4 | 3 | 2 | 1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 |




| 8 FF/4 | 4 FF/3 | 2 FF/2 | 1 FF/1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 |

MODULUS 10 (BCD 8421)

# TELETYPE RECEIVER
## M706

## APPLICATIONS

The M706 converts 5 or 8 bits of serial characters into parallel form and upon a command signal transfers the data into a parallel receiving device.

All buffering, gating, and timing, with the exception of the clock (see Clock), needed for asynchronous operation, device selection, conversion and data transfer, are self-contained on this double height module.

The M706 has the capability of converting either a 5-bit serial input consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial input consisting of 10.0, 10.5, or 11.0 units. This can be done by selecting the correct pins on the socket and tying them together with jumpers on the mating connector.

The serial input must be preceded by a start pulse and followed by two (2) stop pulses (see Timing Diagram). Provision has been made to select the width of the stop pulse from 1.0 units to 1.5 or 2 units long; this also can be done by selecting the proper pins on the socket (see Figure 1).

Besides the above feature, the M706 is equipped with the necessary logic to reject any start pulse that is not greater than ½ unit long, thus eliminating the possibility of false starts. The M706 also provides device selection so that it may be used on the positive bus of the PDP-8/I and the PDP-8/L or an independent teletype transmitter. It can also be used in conjunction with the M707 TTY Transmitter to make up a half duplex system to communicate between TTY and computer (see Figure 3).

When the M706 is used as an independent device and not as an interface to an 8/I or 8/L, the user must supply the correct levels and pulses to ensure proper operation.

NOTE: 1. All pulses must have a pulse width of 50 nsec or greater.
2. All inputs present a one (1) TTL unit load except when noted.
3. All outputs are TTL logic levels and can drive up to 10 unit loads unless otherwise noted.

The outputs will be at a logical 1.

Figure 1 shows the M706 Teletype Receiver used independently of a computer.

In the example shown, the M706 is used to receive serial data from an ASR33 teletype and to transmit in 8-bit parallel code the same data.

The operation of this system starts with a "cue pulse" from the ASR33. This pulse is transmitted via an "OR GATE" to the clear flag 2 input. A high (1) at this point causes a low (0) at pin AE2. Pin AE2 is tied to the reader on input. A low (0) at this point causes the reader run driver to become active, thus starting the reader in the ASR33 to read the tape.

On the first start pulse the active output, which is tied to the flag strobe input, goes low (0), thus causing a high (1) at the strobe flag output. This is tied to the read buffer input through an inverter. Therefore, as long as the

active output is high, no data can be transferred into the receiving device.

On bit 8 of the serial input, the active output goes low (0), causing the read buffer input to go high (1), thus transferring the parallel register into the receiving device.

The K731 Source Module is used to clear the M706 on a power up from the ASR33.

The W994 is used to supply +10 volts needed in the ASR33.

The M401, M405, and the M410 may be used as external clocks (see Logic Handbook).

If the M706 is used for half duplex operation (Figure 2), active (0) should be connected to the wait input of the M707.

**Power Requirements:**
+5 volts, Pin AA2, BA2
Ground AC2, AT1, BC2, BT1
Total Power: +5 volts at 400 ma. (maximum).

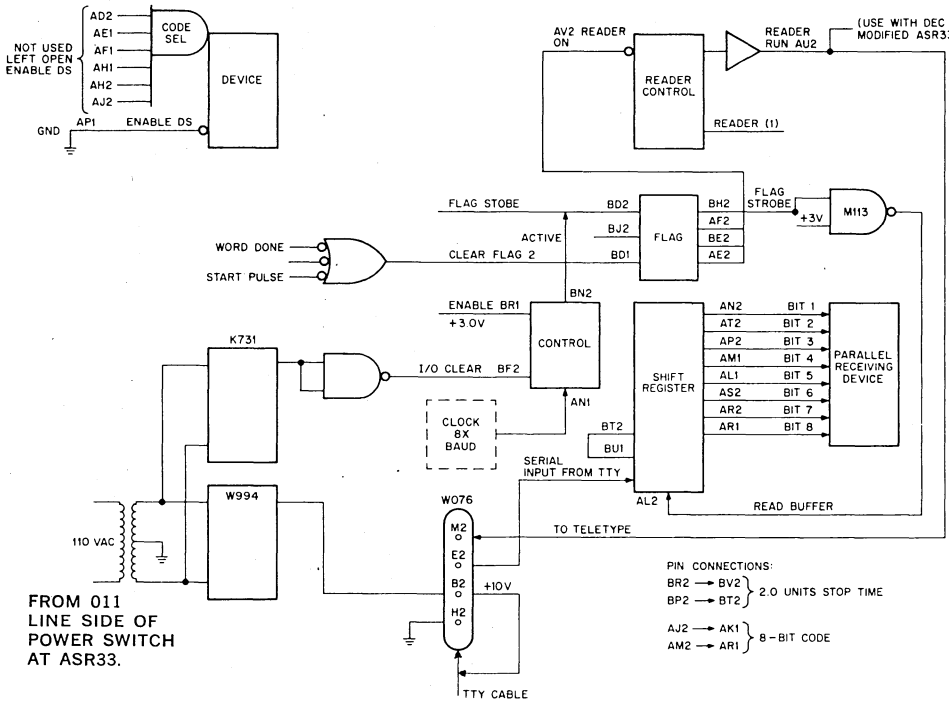



Figure 1

APPLICATIONS: M706 AS AN INTERFACE
BETWEEN ASR33 AND A PARALLEL RECEIVING DEVICE

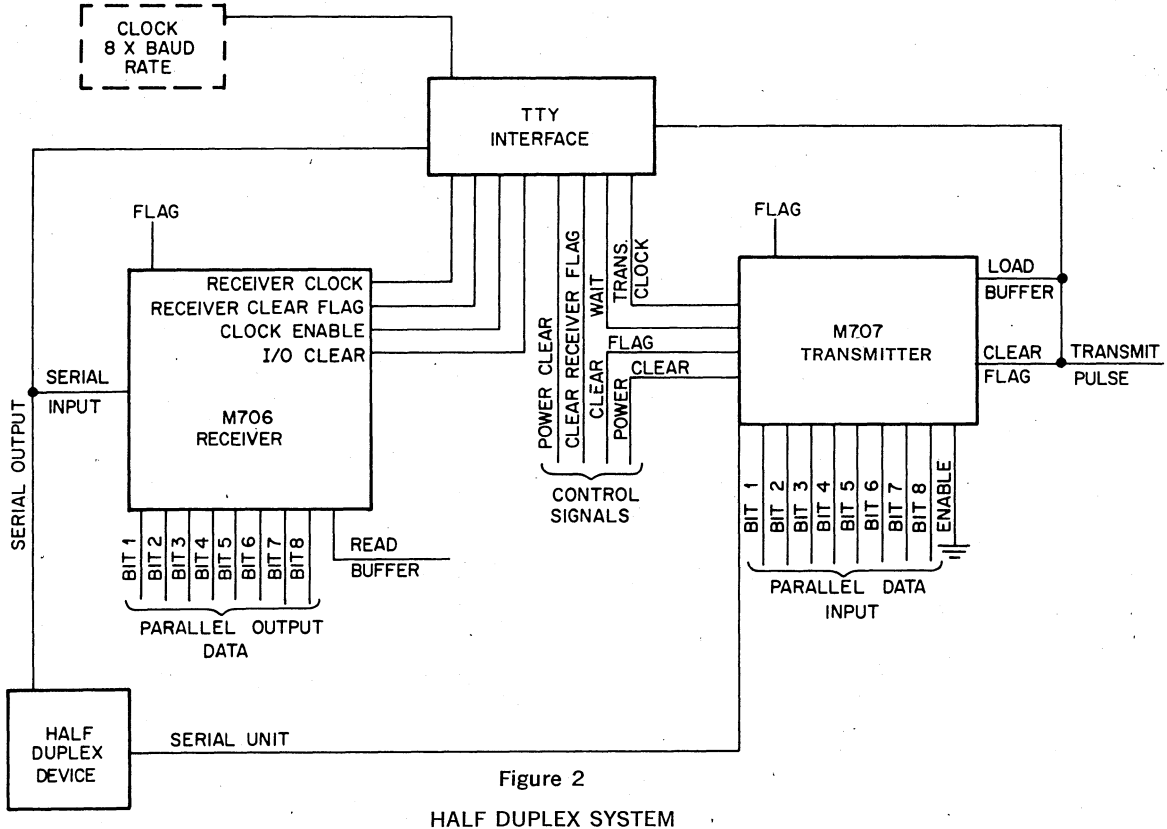



Figure 2

HALF DUPLEX SYSTEM

# TELETYPE TRANSMITTER
## M707

## APPLICATIONS

The M707 Teletype Transmitter is a code converter module used to convert parallel code characters into serial code characters and transmit the data into a serial receiving device.

The buffering, gating, and timing, with the exception of the clock, necessary for an asynchronous operation is located on this double height module.

The M707 is compatible with the M706, having capability of converting either a 5-bit or an 8-bit character through the use of different pin connections on the module. These characters can be assembled into 7.0, 7.5, and 8.0 units for a 5-bit character, and 10.0, 10.5, and 11.0 units for an 8-bit character.

The serial character is transmitted with the start bit first, followed by bit 1 through bit 8 and completed by two (2) stop bits. Through the selection of different pin connections on the module, the stop times can be either 1.0, 1.5, or 2.0 units long (see Timing Diagram).

When the stop bit is put on the serial output, the flag goes low, indicating that a character has been transmitted and that a new parallel character may be loaded.

Another feature included in the M707 is device selection. This allows the module to be used on the positive bus of the PDP-8/I and PDP-8/L and provides the necessary logic so that it can be used in a half duplex system with the M706 Teletype Receiver (see Figure 1).

All inputs present a one (1) TTL unit load unless otherwise noted.

All outputs present a TTL logic level and are capable of driving up to ten unit loads unless otherwise noted.

All pulses require a pulse width of 50 nsec or greater.

**Clock:**
An external frequency source into an input which presents ten (10) unit loads. The frequency output from the clock must be 2 times baud rate, i.e., input bit rate, and may be in the form of either a pulse or a square wave (see M401, M452, M410 in the Logic Handbook).

**Code Selector:**
Can be used for device selection when the BMB 3 - 8 from the positive bus of the PDP-8/I and PDP-8/L are connected to the input. When a positive "AND" occurs at these inputs, the signals flag strobe, load buffer, and clear flag 1 assume their normal functions.

If the code selector is not used, their inputs may be left open and the "Enable DS" line grounded. The input to the code selector must be present 50 nsec prior to any signal that it controls.

**Enable D.S.:**
Should be high or logic (1) when using the code selector and at ground when not using the code selector.

**Flag Strobe:**
A positive pulse or high level at this input causes a negative going pulse at the strobe flag out, provided that the flag is set and that the inputs to the code selector are high. Delay from input to output is 30 nsec maximum.

**Clear Flag 1:**
A high level or positive pulse at this input clears the flag, provided that all code selector inputs are high. When not in use, this input should be held at ground.

**Clear Flag 2:**
When not using the code selector, a negative pulse or low level at this input clears the flag. When not in use, it should be connected to a +3.0 volt source.

**Wait:**
A ground at this input prior to the stop bits of a transmitted character holds transmission of a succeeding character until this line is brought high.
If used in a half duplex system, this line should be connected to the "Active (0)" input of the M706. When not in use, it should be held at +3.0 volts.

**I/O Clear:**
A high level or positive pulse at this point clears the shift register and initializes the state of the control. When not in use or during transmission of a character, this input should be held at ground.

**Bits 1 through 8:**
Contain the 5 or 8 bits of parallel code characters to be converted to serial outputs. A high level at these inputs reflects a logic 1 or mark in the serial output.

When a 5-bit code is used, bit 6 is used as an enable and bits 7, 8, and "Enable" should be at ground.

**Enable:**
Provides the control necessary for transmitter multiplexing. When grounded during a load buffer pulse, it inhibits the transmission of a character.

**Serial Output:**
In an open collector PNP transistor which can drive 20 ma. into any load returned to a voltage between +4 volts and −15 volts. A logical 1 or mark output is +5 volts, and a logical 0 or space output is an open circuit.

Diode protection should be provided for an inducting load. To provide this, a high speed silicon diode is connected from the output to the coil supply voltage. (Cathode to output — anode to supply.)

**Active:**
During the time period from serial start bit to the beginning of the stop bit, the output is high. Output drive is 8 TTL unit loads. This output is used in a half duplex system to obtain special control signals.

**Flag:**
This output goes to ground at the beginning of a stop bit. It drives a 8 TTL unit loads.

**Strobe Flag:**
NAND realization of the inverted flag output and flag strobe. Output can drive 10 TTL unit loads.

**Line:**
This output can drive 10 TTL unit loads and present output signals as logical 1 = +3 volts and logical 0 to ground.

+3 volts: Pin BT1 can drive 10 TTL unit loads at +3 volts.

| | | |
|---|---|---|
| **Power:** | +5 volts at 325 ma. | AA2, BA2 |
| | Ground | AC2, AT1, BC2, BT1 |

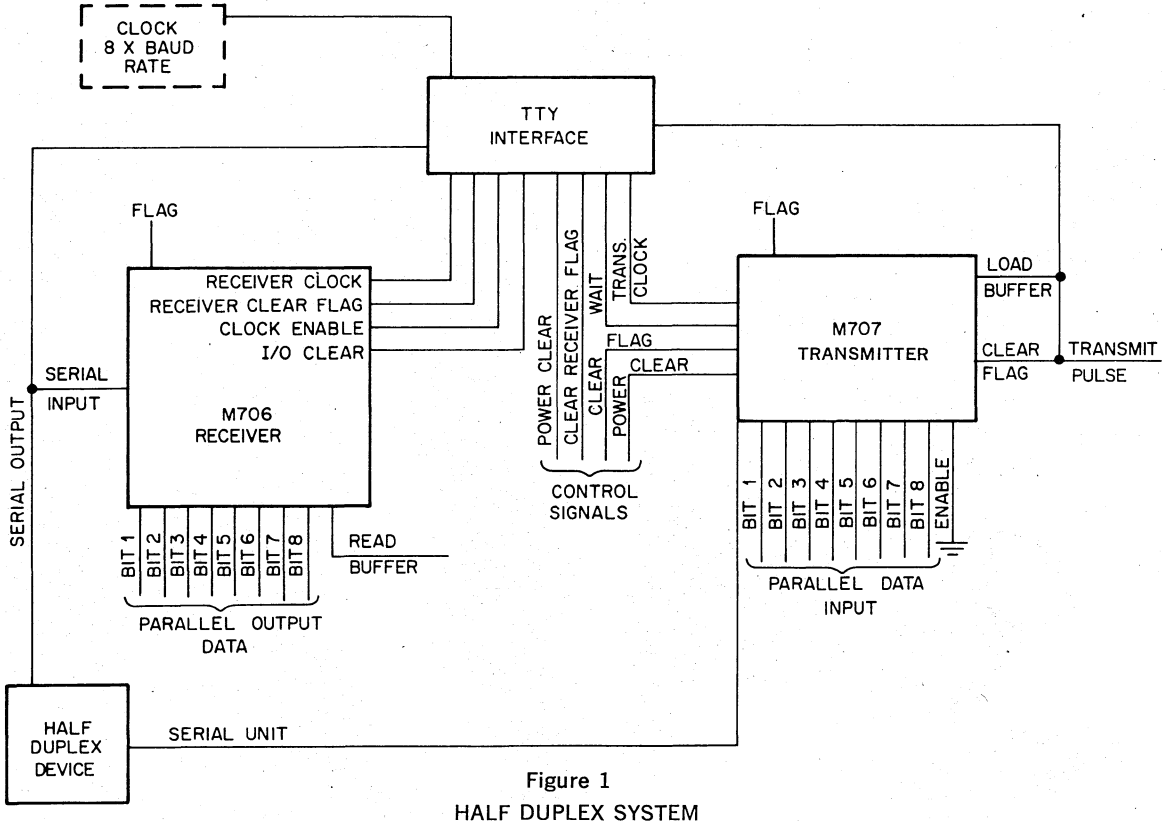



Figure 1
HALF DUPLEX SYSTEM

# BUS INTERFACE
## M730

APPLICATIONS

**Introduction**
The M730 is a double height, single width logic module which provides a complete positive output interface for the Positive Bus PDP-8/I or PDP-8/L. It accepts from the positive bus computer 12 bits of data from the BAC bus, the device selection code from the MB bus, and IOP pulses from the IOP bus. It will send 2 flags to the computer via the skip bus, and will send two pulses (pulse 1 and pulse 2) to the external device. The pulses are variable from 5 - 25 micro-seconds by the use of potentiometers. It will accept done signals from the external device to control the flags. The M730 also sends 12 bits of data to the external device.

**Flag Control**
Setting Flag 1 or Flag 2 causes an interrupt which comes from an open collector NPN transistor to the positive bus computer in the form of a ground signal. Skip on Flag 1 with IOT 6XY1. Skip on Flag 2 with IOT 6XY3. The skip output is also an open collector NPN transistor which, when asserted, sends a ground signal to the positive bus computer. Both skip and interrupt outputs are open collector NPN transistors that can be tied directly to the skip and interrupt bus of the positive bus computer. Flag 1 and Flag 2 outputs are available as M Series TTL outputs and as noted are ground when true. Flag 1 is set by done 1− and done 1+ from the external device. In order to set Flag 1, done 1− must go to ground and done 1+ must go to at least +2.5 v. If desired, one can tie done 1+ to +3VDC and set Flag 1 by issuing a negative pulse or level at done 1−. To set Flag 2 use done 2− and done 2+, the same as Flag 1− and Flag 1+. Flag 1 and Flag 2 can be cleared by initialize or by IOT 6XY2.

| Signal | Logic Level |
|---|---|
| Device Selector Signals | M Series Logic levels (TTL) |
| 12 Bit Storage Register | From Computer to Device (TTL) |
| done 1, done 2 | TTL |
| Flag 1, Flag 2 | TTL |
| Pulse 1, Pulse 2 | Positive |

**Device Selector Control:**
The code selector accepts M Series levels BMB 3-8. When the Code Select Card Gate is met (depending on the code wired in) the Option Select line is a +3 v. M Series level. The code select by BMB 3-8 can be bypassed by putting a ground on the enable line, which will also make the Option Select Line go to +3 v. The Option Select Line acts as an enable to allow gating of M

Series pulses IOP 1, 2, and 4 and M Series levels BMB 9 (1), BMB 10 (1), and BMB 11 (1) to issue the IOT's listed below depending on which gates are met.

| Mnemonic | On IOP | Operation |
|---|---|---|
| 6XY1 | 1 | Skip on Flag 1 |
| 6XY2 | 2 | Clear Flags 1 and 2 |
| 6XY3 | 1 | Skip on Flag 2 |
| 6XY4 | 4 | Issue Pulse 1 |
| 6XY5 | 4 | Clear Pulse 1− and Pulse 1+ when jumper A & C are in |
| 6XY6 | 4 | Load the BAC into the 12 Bit Storage Register |
| 6XY7 | 4 | Issue Pulse 2 |

**Timing Generator Control:**
Upon issuing IOT 6XY4 Pulse 1− and Pulse 1+ will receive a pulse. Note that Pulse 1− and Pulse 1+ are the inverse of each other. Pulse duration can be from 5 $\mu$s to 25 $\mu$s depending on the setting of the potentiometer mounted on the board. The amplitude of the pulse out can be from 0 v. to +20 v., depending on the clamp on the open collector NPN transistor output on the Data Lines.

**SPECIFICATIONS:**
**Inputs**
Done 1−, Done 1+, Done 2−, and Done 2+ present one TTL unit load at ground and are protected for input voltage between −20 to +20 volts and have an input threshold at +1.5 volts.

Code Select, Initialize, and BMB 9-11 are M Series inputs and each draw 1 unit load (1.6 ma). All other inputs are M Series inputs and draw 2 unit loads each.

**Outputs**
All outputs including computer inputs drive 30 ma non-inductive at ground with a maximum positive output voltage of +20 volts. The outputs are driven by an open collector NPN transistor. Pulse 1 and Pulse 2 outputs are adjustable from 5 $\mu$s to 25 $\mu$s with a recovery time of 40 $\mu$s to 250 $\mu$s. Note that data lines and pulse output lines have to be diode protected if driving an inductive load.

| Power | Current |
|---|---|
| +5v Pin AA2, BA2 | 500 ma (max.) |

Grd Pin AC2, AT1
BC2, BT1

Some care must be taken when using the M730 to avoid overloading the bus. Normally, the bus can drive 64 devices or ports. An unbuffered M730 presents to the bus a load which is equivalent to ten normal ports.

A large port capability, using the M730, can be realized by buffering it with the M101, using the Option Select Line as the enable for the M101. In this

configuration each M730 and M101 combination looks to the bus like 2.6 ports. Use of this method allows 25 M730's on the bus, rather than six.

On the following few pages are shown a configuration for each method.

## JUMPER NOTES

A & C in — Outputs BD2, BE2 at asserted levels from IOTXY4 until IOTXY5.

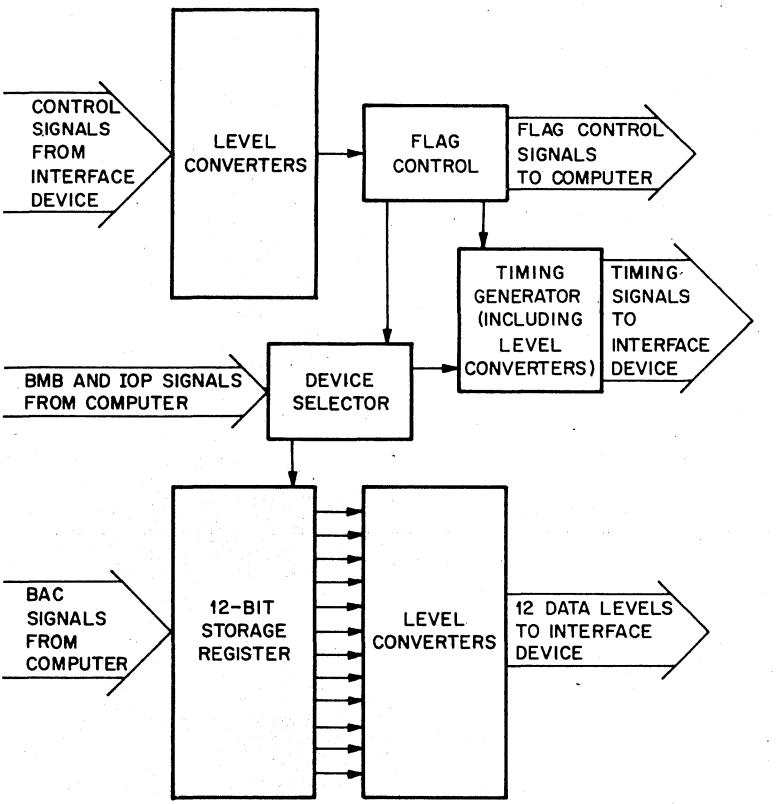
A & B in — Outputs BD2, BE2 at asserted levels from IOTXY4 until Flag 1 is set by AND of data on inputs AR2, AS2.

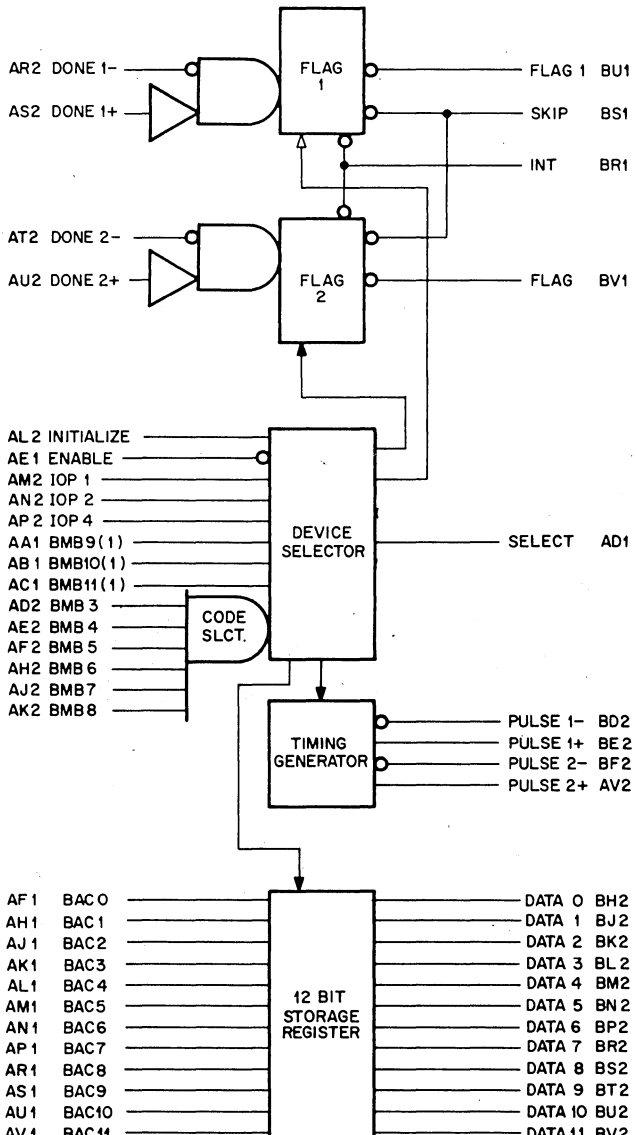
D & F — Outputs BF2, AV2 at asserted levels from IOTXY7 until Flag 2 is set by AND of data on inputs AT2, AU2.

D & E — Outputs BF2, AV2 at asserted levels as using D & F until Flag 1 is set.

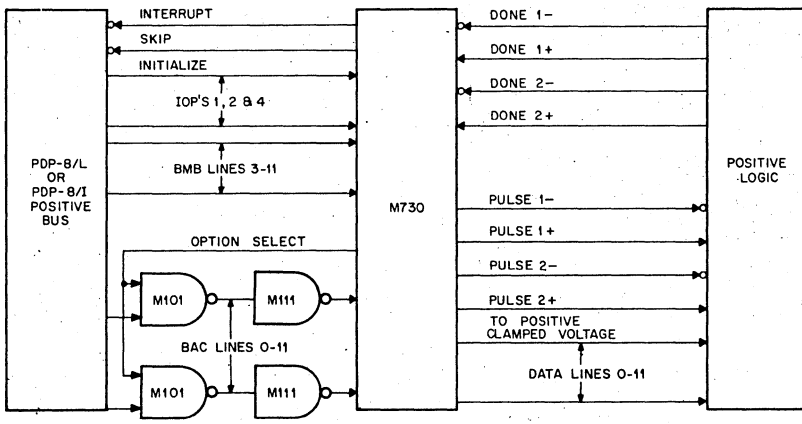
Pulse widths presently 5 $\mu$s-25 $\mu$s recovery time 40 $\mu$s-250 $\mu$s.

All units when used on I/O bus require M907 or equivalent diode undershoot protection.

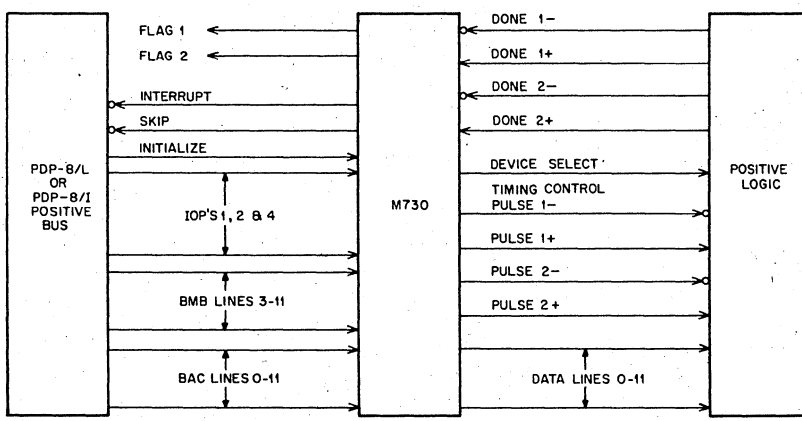

CONTROL SIGNALS FROM INTERFACE DEVICE
LEVEL CONVERTERS
FLAG CONTROL
FLAG CONTROL SIGNALS TO COMPUTER
TIMING GENERATOR (INCLUDING LEVEL CONVERTERS)
TIMING SIGNALS TO INTERFACE DEVICE
BMB AND IOP SIGNALS FROM COMPUTER
DEVICE SELECTOR
BAC SIGNALS FROM COMPUTER
12-BIT STORAGE REGISTER
LEVEL CONVERTERS
12 DATA LEVELS TO INTERFACE DEVICE




M730 POSITIVE OUTPUT INTERFACE FOR POSITIVE BUS 8/I OR 8/L




USE OF M730 USING M101 & M111




USE OF M730 ALONE

After the modules are flow-soldered, they undergo a visual inspection to insure that all solder points and runs are properly made. If needed, additional solder is added.

# BUS INTERFACE
## M731

**APPLICATIONS**

The M731 is a double height, single width logic module which provides a negative output interface for the positive bus PDP-8/I or PDP-8/L. It receives from the positive bus computer 12 bits of data from the BAC bus, and IOP pulses from the IOP bus, and sends 2 flags to the computer via the skip bus, as well as two pulses (pulse 1 and pulse 2) to the external device to control the flags. The M731 also sends 12 bits of data to the external device.

**Flag Control**
Setting flag 1 or flag 2 causes an interrupt which comes from an open collector NPN transistor to the positive bus computer in the form of a ground signal. Skip on flag 1 with IOT 6XY1.* Skip on flag 2 with IOT 6XY3. The skip output is also an open collector NPN transistor which, when asserted, sends a ground signal to the positive bus computer. Both skip and interrupt outputs are open collector NPN transistors that can be tied directly to the skip and interrupt bus of the computer. Flag 1 and flag 2 outputs are available and are at ground when true. Flag 1 is set by done 1− and done 1+ from the external device. In order to set flag 1, done 1− must be more negative than −2 volts and done 1+ must be at ground. If desired, one can tie done 1+ to ground and set flag 1 by issuing a negative pulse or level at done 1−. To set flag 2, use done 2− and done 2+ in the same way as flag 1− and flag 1+. Flag 1 and flag 2 may be cleared by Initialize or by IOT 6XY2.

| Signal | Logic Level |
|---|---|
| Device selector signals | M Series logic levels (TTL) |
| 12-bit storage register input | BAC-TTL from computer |
| 12-bit storage register output | Data 0-11 (Negative) Open Collector |

NOTE: 6XY1 indicates a selected device code, i.e., 6031, etc.

| | |
|---|---|
| Done 1, done 2 | Negative |
| Flag 1, flag 2 | TTL |
| Pulse 1, pulse 2 | Negative |
| Skip, Interrupt Reg. | Open collector positive |

**Device Selector Control**
The code selector accepts M Series levels for BMB 3-8 inputs. When the Code Select Card Gate input requirements are met (depending on the code wired in), the Option Select line will be at a +3 v. level. (The code select inputs BMB 3-8 can be bypassed by putting an M Series ground on the enable line, which will also make the Option Select Line go to +3 v.) The Option Select Line acts as an enable to allow gating of M Series pulses IOP 1, 2, and 4, and M Series levels BMB 9 (1), BMB 10 (1), and BMB 11 (1) to issue the IOT's listed below, depending on which gates are met.

**Specifications**

**Inputs**

Done 1−, Done 1+, Done 2−, Done 2+

| | Maximum | Minimum |
|---|---|---|
| Logical 0 (Gnd) | +2 v. | − 1 v. |
| Logical 1 (−3 v.) | −2 v. | −20 v. |
| Current required at ground | 5 ma. | |
| Threshold voltage | | − 1.5 v. |

Code Select, Initialize, & BMB 9-11 are M Series inputs and each line draws 1 unit load (1.6 ma). All other inputs are M Series levels and draw 2 unit loads each.

**Outputs**

Data 0-11 and pulse 1 and 2 outputs drive 30 ma. non-inductive at ground with a maximum negative output voltage of −20 volts, provided by an open collector PNP transistor. Pulse 1 and Pulse 2 outputs are adjustable from 5 μs to 25 μs with a recovery time of 40 μs to 250 μs. Computer inputs such as skip and interrupt can drive 30 ma. at ground through an open collector NPN transistor. Note that data lines and pulse output lines have to be diode protected if driving an inductive load.

| **Power** | **Current** |
|---|---|
| +5 v. DC ± 5% Pin AA2, BA2 | 500 ma. (Max.) +5 v. DC |
| −15 v. DC ±10% Pin AB2, BB2 | 50 ma. −15 v. DC |

GRD Pin AC2, AT1, BC2, BT1

Some care must be taken when using the M731 to avoid overloading the bus. Normally, the bus can drive 64 devices or ports. An unbuffered M731 presents to the bus a load which is equivalent to ten normal ports.

A large port capability, using the M731, can be realized by buffering it with the M101 using the Option Select line as the enable for the M101. In this configuration each M731 and M101 combination looks to the bus like 2.6 ports. Use of this method allows 25 M731's on the bus, rather than six.

Figure 3 and 4 show a configuration for each method which is listed above.

| Mnemonic | On IOP | Operation |
|---|---|---|
| 6XY1 | 1 | Skip on flag 1 |
| 6XY2 | 2 | Clear flags 1 and 2 |
| 6XY3 | 1 | Skip on flag 2 |
| 6XY4 | 4 | Issue on pulse 1 |
| 6XY5 | 4 | Clear pulse 1− and pulse 1+ when jumper A+C are in |
| 6XY6 | 4 | Load the BAC into the 12-Bit Storage Register |
| 6XY7 | 4 | Issue pulse 2 |

**Timing Generator Control**

Upon issuing IOT 6XY4 Pulse 1− and Pulse 1+ will receive a pulse. Note that Pulse 1− and Pulse 1+ are the inversions of each other. Pulse duration can be from 5 μs to 25 μs depending on the setting of the potentiometer mounted on the board. The amplitude of the pulse out can be from Ov. to −20v. depending on the clamp on the open collector PNP transistor output.

Issuing IOT 6XY7 will cause Pulse 2− and Pulse 2+ to receive a pulse. The same characteristics hold true here as for Pulse 1− and Pulse 1+.

**12-BIT STORAGE REGISTER CONTROL**

Issuing of IOT 6XY6 will cause the M Series level BAC bits 0-11 from the computer to be loaded into the 12-Bit Storage Register. This information is now on the data lines 0-11. It is in the form or levels of negative logic and thus can readily be interfaced to a negative logic system. The data outputs are levels from 0 v. to −20 v. depending on the clamp on the open collector PNP transistor output on the Data Lines.

JUMPER NOTES

A & C in — Outputs BD2, BE2, at asserted levels from IOTXY4 until IOTXY5.
A & B in — Outputs BD2, BE2, at asserted levels from IOTXY4 until flag 1 is set by AND of data on inputs AR2, AS2.
D & F — Outputs BF2, AV2 at asserted levels from IOTXY7 until flag 2 is set by AND of data on inputs AT2, AU2.
D & E — Outputs BF2, AV2, at asserted levels as using D & F until flag 1 is set.

Pulse widths presently 5 $\mu$s-25 $\mu$s recovery time 40 $\mu$s-25 $\mu$s.

All units when used on I/O bus require M907 or equivalent diode undershoot protection.

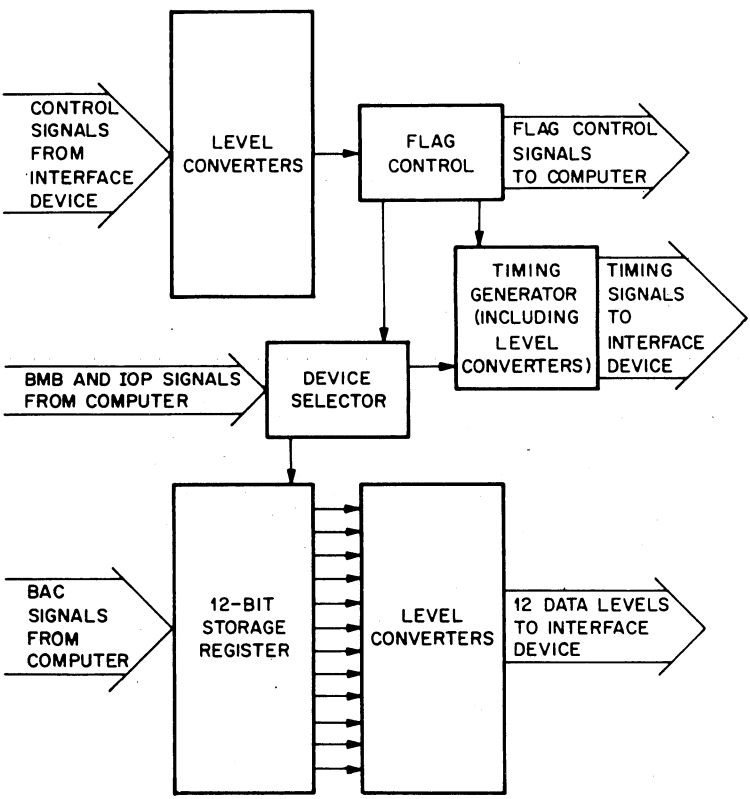



Figure 1. PDP-8/I, PDP-8/L, I/O OUTPUT BUS INTERFACE MODULE TYPE M731

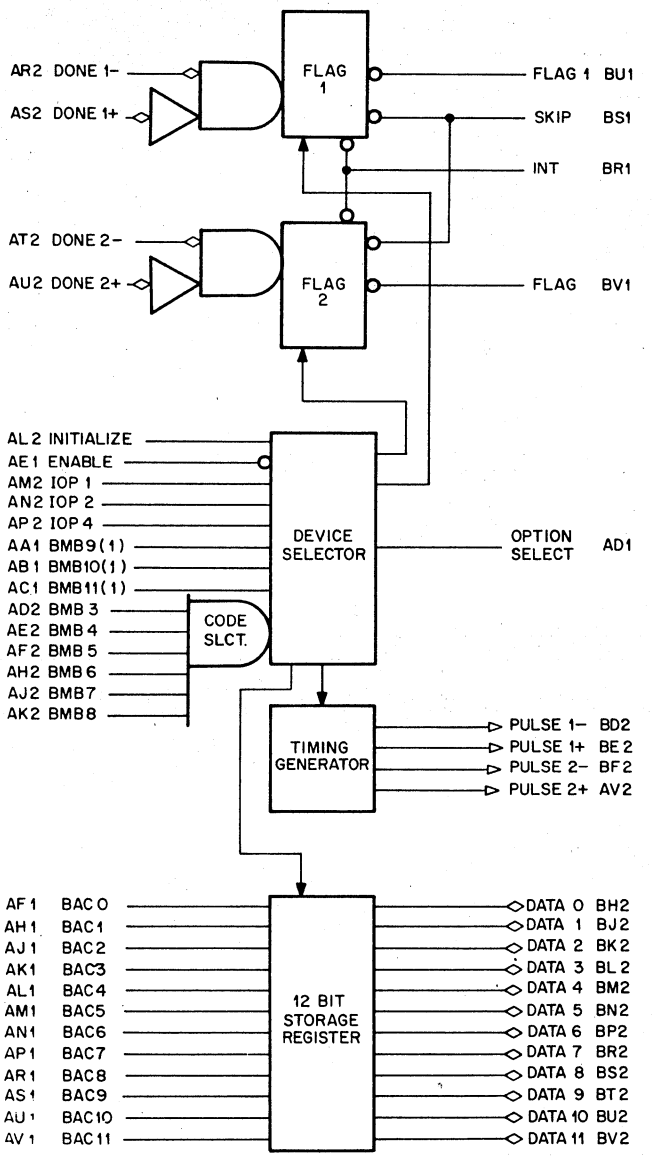



Figure 2. M731 8/I BUS-NEGATIVE OUTPUT INTERFACE

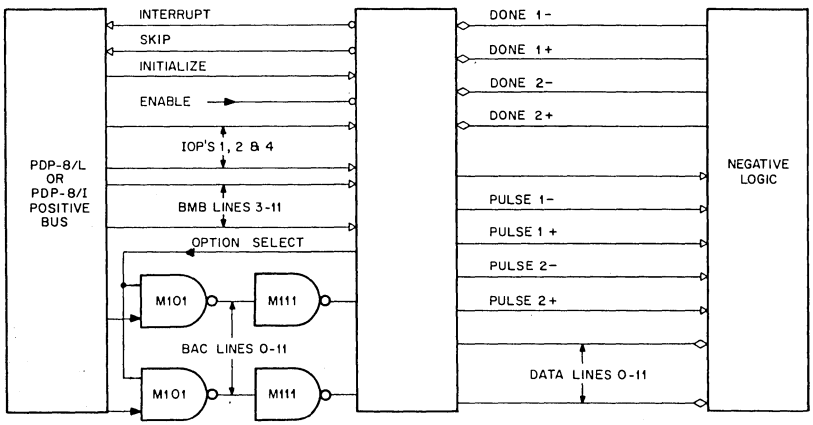



Figure 3. USE OF M731 USING M101 & M111

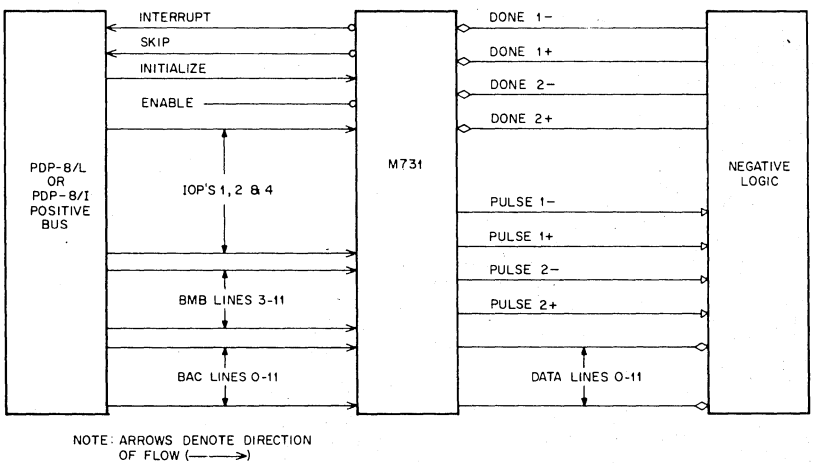



Figure 4. USE OF M731 ALONE

# POSITIVE INPUT BUS INTERFACE
## M732

APPLICATIONS

The M732 is a double height, single width logic module which provides a complete positive input interface for the positive bus PDP-8/I or PDP-8/L. It receives 12 parallel bits of data from the external device and transmits 12 bits of data from the storage register to the computer via the BAC bus under computer control. It accepts from the positive bus computer the device selection code from the MB bus, and IOP pulses from the IOP bus. Two separate flags can be generated and sent to the computer via the skip bus, also two timing pulses (pulse 1 and pulse 2) can be sent to the external device. The timing pulses are variable from 5-25 microseconds by the use of potentiometers mounted on the module. Done signals are accepted from the external device to control the flags. The basic restriction on the device or system to be interfaced is that it must have a data transfer rate of less than 20 KHz.

**Flag Control**
Setting Flag 1 or Flag 2 causes an interrupt which comes from an open collector NPN transistor to the positive bus computer in the form of a ground signal. Skip on Flag 1 with IOT 6XY1. Skip on Flag 2 with IOT 6XY3. The skip output is also an open collector NPN transistor which, when asserted, sends a ground signal to the positive bus computer. Both skip and interrupt outputs are open collector NPN transistors that can be tied directly to the skip and interrupt bus of the positive bus computer. Flag 1 and Flag 2 ouputs are available as M Series TTL outputs and as noted are ground when true. Flag 1 is set by done 1− and done 1+ from the external device. In order to set Flag 1, done 1− must go to ground and done 1+ must go to at least +2.5v. If desired, one can tie done 1+ to +3v. and set Flag 1 by issuing a negative pulse or level at done 1−. To set Flag 2, use done 2− and done 2+, the same as Flag 1− and Flag 1+. Flag 1 and Flag 2 can be cleared by Initialize or by IOT 6XY2.

| Signal | Logic Level |
|---|---|
| Device selector signals | M Series logic levels (TTL) |
| 12-Bit Storage Register | From computer to device (TTL) |
| Done 1, Done 2 | TTL |
| Flag 1, Flag 2 | TTL |
| Pulse 1, Pulse 2 | Positive |

**Device Selector Control**
The Code Select Gate accepts M Series levels BMB bits 3-8. When the Code Select Gate is met (depending on the code wired in) the Option Select line is at a +3 volt level. The Code Select Gate can be bypassed by inserting a ground on enable line. This will also make the option select line go to +3 volts. The Option Select Line acts as an enable to allow gating of IOP pulses

1, 2, and 4 with BMB 9 (1), BMB 10 (1), and BMB 11 (1) to issue the IOT's listed below depending on which gates are conditioned.

| Mnemonic | On IOP | Operation |
|---|---|---|
| 6XY1 | 1 | Skip on flag 1 |
| 6XY2 | 2 | Clear flags 1 and 2 |
| 6XY3 | 1 | Skip on flag 2 |
| 6XY4 | 4 | Issue pulse 1 |
| 6XY5 | 4 | Clear pulse 1− and pulse 1+ when jumpers A & C are inserted |
| 6XY6 | 2 | Clear AC |
| 6XY6 | 4 | Read AC0-AC11 from the M624 into the accumulator of the computer. |
| 6XY7 | 4 | Issue pulse 2 |

**Timing Generator Control:**
Upon issuing IOT 6XY4 Pulse 1− and Pulse 1+ will receive a pulse. Note that Pulse 1− and Pulse 1+ are the inverse of each other. Pulse duration can be from 5 $\mu$s to 25 $\mu$s, depending on the setting of the potentiometer mounted on the board. The amplitude of the pulse out can be from 0 v. to +20 v. depending on the clamp on the open collector NPN transistor output. Issuing IOT 6XY7 will cause Pulse 2− and Pulse 2+ to receive a pulse. The same characteristics hold true here as for Pulse 1− and Pulse 1+.

**12-Bit Storage Register Control:**
Upon setting the flag 2 by the done 2 signal, data 0 through data 11 is read into the storage register. The positive logic signals being interfaced on the data lines can be from 0 v. to +20 v. levels. A ground or 0 v. level on the data line read into the storage register input yields a +3 v. level on the output (AC). A +3 v. signal or larger up to +20 v. read into the storage register input from the data lines will yield a ground level out of the storage register on the AC lines. For assertion of a one into the computer, the appropriate data lines has to be at least +2.5 or greater, up to +20 v. The storage register output AC0 through AC11 can be read into the accumulator using an M624 Bus Driver module and the data out strobe IOT 6XY6.

**SPECIFICATIONS:**
**Inputs**
All inputs appear as M Series TTL loads. Inputs present 2 unit loads except for the following inputs, which present only one unit load: Code Select, Initialize, BMB 9-11, and data 0-11. Data inputs expect a logical 0 of 0, +1, −3 and a logical 1 of +3, +17, −1 volts.

**Outputs**
All outputs drive 30 ma. at ground through NPN transistors except AC0-AC11, Select (1), Flag 1 (0), and Flag 2 (0). AC0-AC11 must be connected to the M624 module and then will be capable of driving 100 ma. at ground. Select (1), Flag 1 (0), and Flag 2 (0) outputs are normal TTL levels with output drive capability in unit loads of respectively 1, 7, and 7.

| Power | Current |
|---|---|
| +5 v. ±5% AA2, BA2 | 500 ma. (max.) |
| GRD AC2, BC2 | |
| AT1, BT1 | |

JUMPER NOTES

A & C in — Outputs BD2, BE2 at asserted levels from IOTXY4 until IOTXY5.

A & B in — Outputs BD2, BE2 at asserted levels from IOTXY4 until Flag 1 is set by AND of data on inputs AR2, AS2.

D & F — Outputs BF2, AV2 at asserted levels from IOTXY7 until Flag 2 is set by AND of data on inputs AT2, AU2.

D & E — Outputs BF2, AV2 at asserted levels as using D & F until Flag 1 is set.

Pulse widths presently 5 $\mu$s-25 $\mu$s recovery time 40$\mu$s-25 $\mu$s.

All units when used on I/O bus require M907 or equivalent diode undershoot protection.

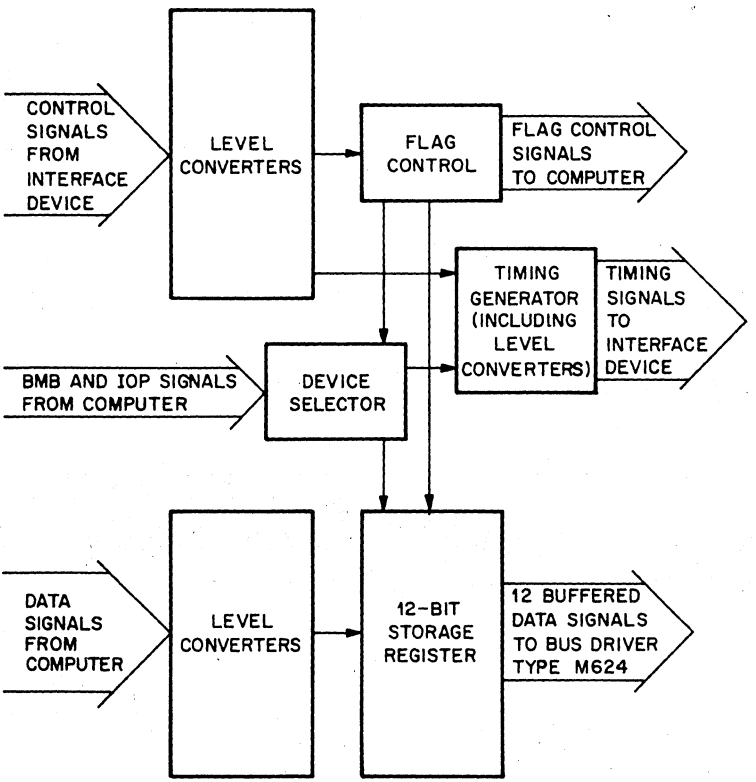



Figure 1. PDP-8/I, PDP-8/L, I/O INPUT BUS INTERFACE MODULE TYPE M732

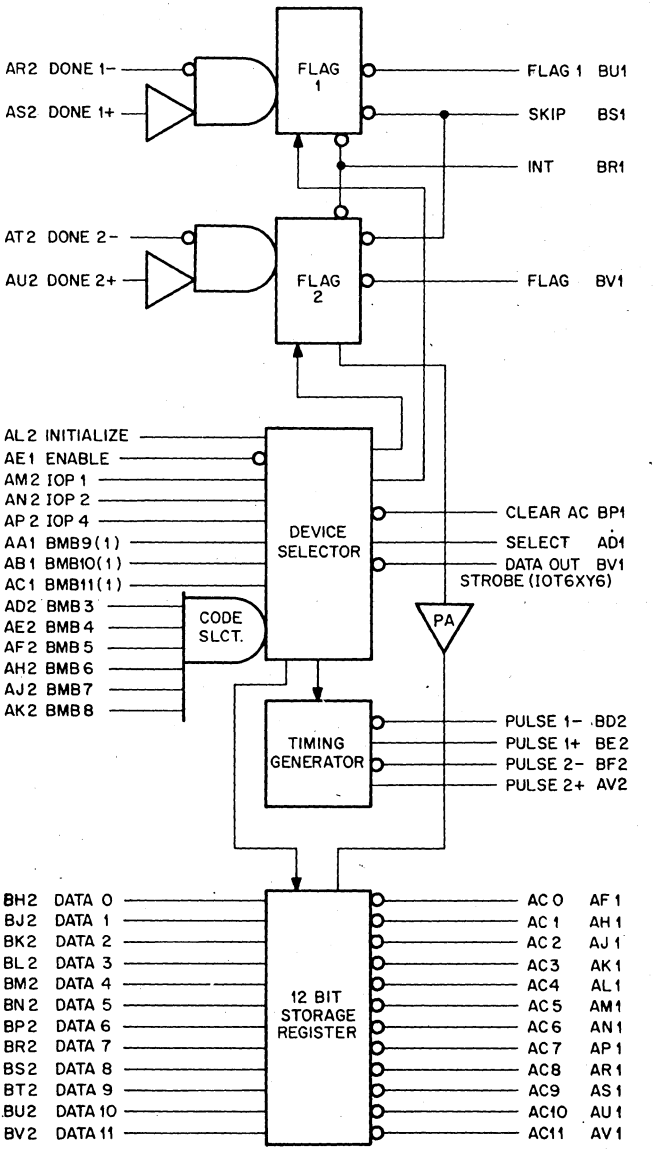



Figure 2. M732 8/I BUS — POSITIVE INPUT INTERFACER TTL OUTPUT LEVELS

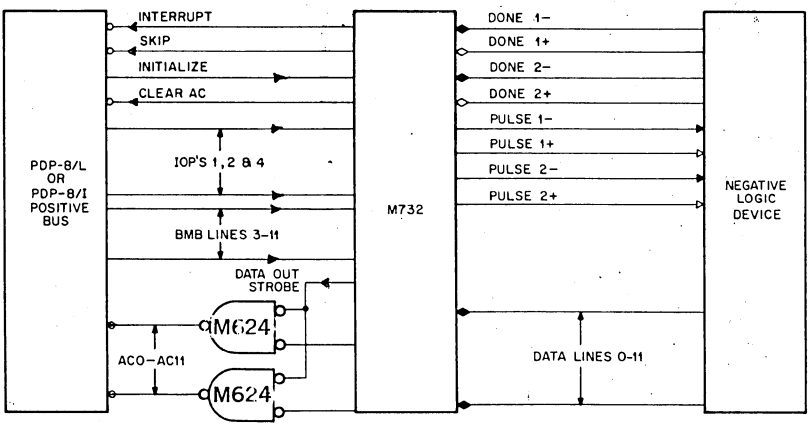



Figure 3.
USE OF M732

# BUS INTERFACE
## M733

APPLICATIONS

The M733 8/I Bus Negative Input Interface Module is a double height, single width module. It provides extremely flexible interface control logic to connect devices, systems, and instruments to the input half of the programmed I/O transfer bus of either a positive bus PDP-8/I or a PDP-8/L computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to transmit data to that computer can to a large degree be interfaced by the M733, provided that the information being transmitted to the computer is a negative voltage. Basic restrictions on the device or system to be interfaced are simply that it transmit data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20 KHz. Complete interfaces to such peripheral gear as card readers and other repetitive devices are possible using the M733; however, part of the controlling functions, such as counting, etc., must be performed by computer software.

**Flag Control**

Flag 1 is set by done 1− and done 1+ (either pulses or levels from device indicating a completion of operation). In order to set flag 1, done 1− must be more negative than minus 2 v. and done 1+ must be at ground. If desired, done 1+ can be tied to ground and flag 1 can then be set by receiving a negative pulse or level at done 1−. To set flag 2, use done 2− and done 2+. Flag 1 and flag 2 can be cleared by an initialize signal from the computer or by IOT 6XY2. The setting of flag 1 or flag 2 causes an interrupt signal (ground level) to be shipped over the I/O bus to the computer. After recognizing the interrupt, the computer can skip on flag 1 or flag 2 with IOT 6XY1 or IOT 6XY3 in that order if the appropriate flag is set. The skip signal is also shipped over the I/O bus to the computer. It is also ground for assertion.

**Device Selector Control**

The Code Select Gate accepts M Series levels BMB bits 3-8. When the Code Select Gate is met (depending on the code wired in), the option select line is at a +3 volt level. The Code Select Gate can be bypassed by inserting a ground on the enable line. This will also make the Option Select line go to +3 volts. The Option Select line acts as an enable to allow gating of IOP

pulses 1, 2, and 4 with BMB 9 (1) and BMB 10 (1) and BMB 11 (1) to issue the IOT's listed below, depending on which gates are conditioned.

| Mnemonic | On IOP | Operation |
|---|---|---|
| 6XY1 | 1 | Skip on flag 1 |
| 6XY2 | 2 | Clear flags 1 and 2 |
| 6XY3 | 1 | Skip on flag 2 |
| 6XY4 | 4 | Issue pulse 1 |
| 6XY5 | 4 | Clear pulse 1− and pulse 1+ when jumpers A & C are inserted |
| 6XY6 | 2 | Clear AC |
| 6XY6 | 4 | Read AC0-AC11 from the M624 into the accumulator of the computer |
| 6XY7 | 4 | Issue pulse 2 |

**Timing Generator Control**

Upon issuing IOT 6XY4 pulse 1− and pulse 1+ will receive a pulse. Note that pulse 1− and pulse 1+ are the inverse of each other. Pulse duration can be from 5 $\mu$s to 25 $\mu$s, depending on the setting of the potentiometer mounted on the board. The amplitude of the pulse out can be from 0 v. to −20 v. depending on the clamp on the open collector PNP transistor output. Issuing IOT 6XY7 will cause pulse 2− and pulse 2+ to receive a pulse. The same characteristics hold true here as for pulse 1− and pulse 1+.

**12-Bit Storage Register Control**

Upon setting of flag 2 by the done 2 signal, data 0 through data 11 is read into the storage register. The negative logic signals being interfaced on the data lines can be from o v. to −20 v. levels. A ground or 0 v. level on the data line read into the storage register input yields a +3 v. level on the output $\overline{AC}$. A −2 v. signal or larger, up to −20 v., read into the storage register input from the data lines will yield a ground level out of the storage register on the AC lines. For assertion of a one into the computer, the appropriate data line has to be at least −2 v. or greater, up to −20 v. The storage register output $\overline{AC0}$ through $\overline{AC11}$ can be read into the accumulator using an M624 Bus Driver module and the data out strobe IOT 6XY6.

**Specifications**

**Inputs**

Done 1−, Done 1+, Done 2−, Done 2+

| Data 0 through Data 11 | Maximum | Minimum |
|---|---|---|
| Logical 0 (gnd) | +2 v. | −1 v. |
| Logical 1 (−3 v.) | −2 v. | −20 v. |
| Current required at ground | 5 ma. | |
| Threshold Voltage | | −1.5 v. |

All other inputs expect standard M Series levels or pulses and present 2 unit loads, except for the following inputs, which present 1 unit load — Code Select, Initialize, and BMB 9-11.

**Outputs**
All outputs drive 30 ma. at ground. Outputs to the input system are open collector PNP transistors with a maximum output voltage rate of −20 volts.

| **Power** | **Current** |
|---|---|
| +5 v. ±5% | 500 ma. (Max.) |
| −15 v. ±10% | 125 ma. (Max.) |

220

JUMPER NOTES

A & C in — Outputs BD2, BE2 at asserted levels from IOTXY4 until IOTXY5.

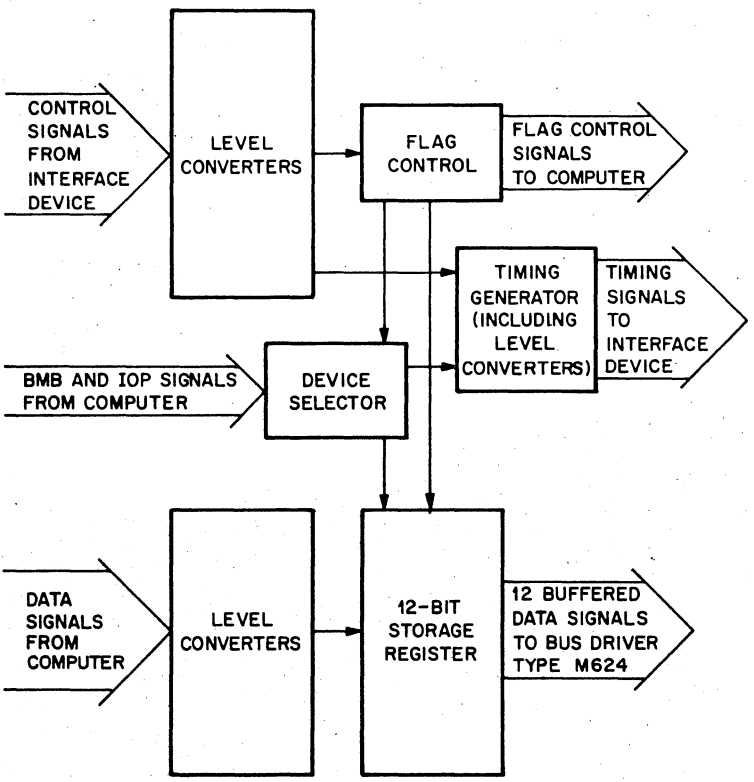
A & B in — Outputs BD2, BE2 at asserted levels from IOTXY4 until flag 1 is set by AND of data on inputs AR2, AS2

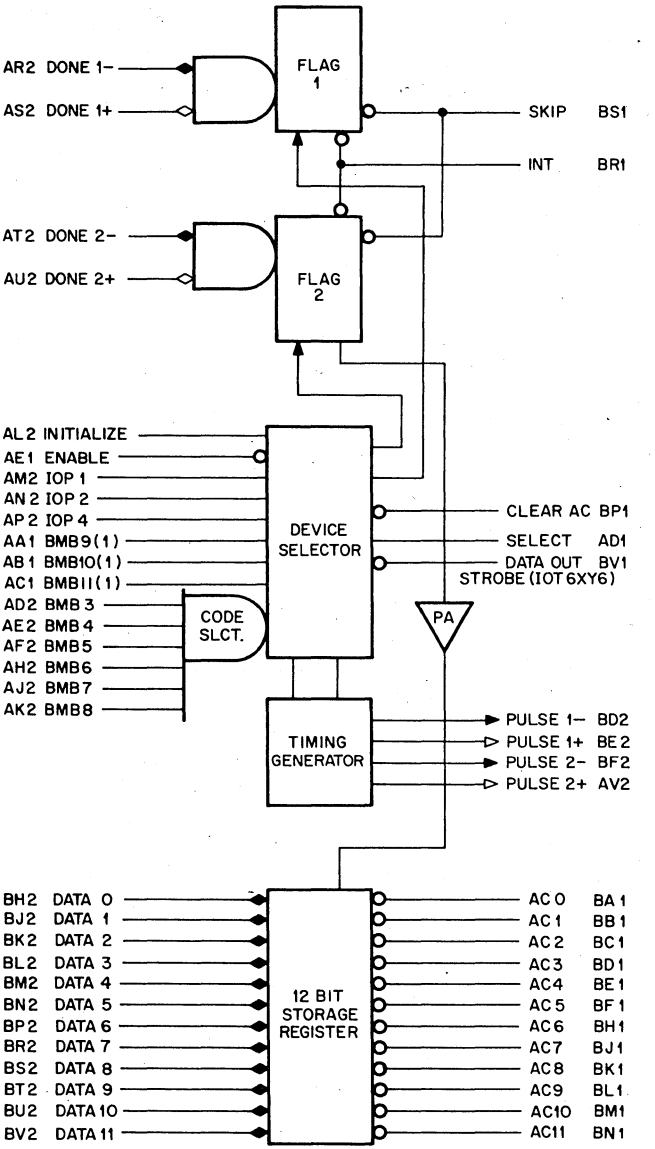
D & F — Outputs BF2, AV2 at asserted levels from IOTXY7 until flag 2 is set by AND of data on inputs AT2, AU2.

D & E — Outputs BF2, AV2 at asserted as using D & F until flag 1 is set.

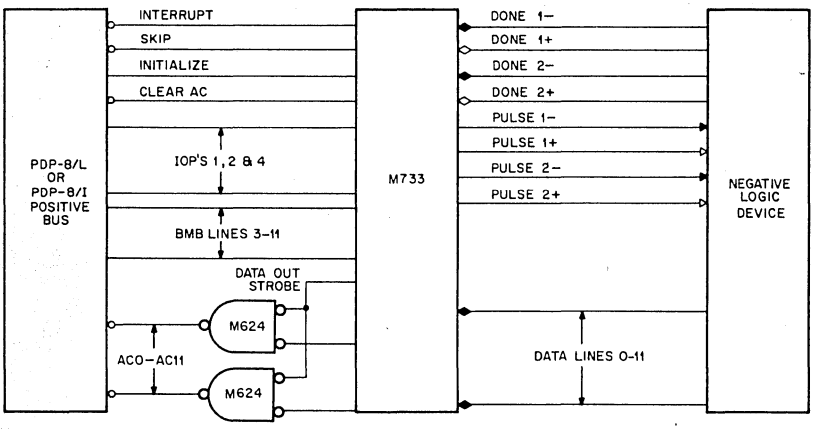
Pulse widths presently 5 μs-25 μs recovery time 40 μs-250 μs.

All units when used on I/O bus require M907 or equivalent diode undershoot protection.


CONTROL SIGNALS FROM INTERFACE DEVICE
LEVEL CONVERTERS
FLAG CONTROL
FLAG CONTROL SIGNALS TO COMPUTER
TIMING GENERATOR (INCLUDING LEVEL CONVERTERS)
TIMING SIGNALS TO INTERFACE DEVICE
BMB AND IOP SIGNALS FROM COMPUTER
DEVICE SELECTOR
DATA SIGNALS FROM COMPUTER
LEVEL CONVERTERS
12-BIT STORAGE REGISTER
12 BUFFERED DATA SIGNALS TO BUS DRIVER TYPE M624




M733 8/I NEGATIVE INPUT INTERFACE


PDP-8/L
OR
PDP-8/I
POSITIVE
BUS
INTERRUPT
SKIP
INITIALIZE
CLEAR AC
IOP'S 1, 2 & 4
BMB LINES 3-11
DATA OUT
STROBE
M624
ACO-AC11
M624
M733
DONE 1-
DONE 1+
DONE 2-
DONE 2+
PULSE 1-
PULSE 1+
PULSE 2-
PULSE 2+
DATA LINES 0-11
NEGATIVE
LOGIC
DEVICE

USE OF M733

# M734-INPUT MULTIPLEXING FROM THREE SEPARATE 12-BIT DEVICES, AND PARALLEL LOADING OF 20-BIT WORD INTO POSITIVE BUS PDP-8/I, 8/L

## APPLICATIONS

Figure 1 shows the M734 connected as an interface between two (2) 10-bit A/D Converters, one (1) 12-bit digital clock, and a Positive Bus PDP-8/I, 8/L.

When an "AND" condition occurs at the inputs to the code selector by wiring the proper BMB to form the selected code, i.e., when the BMB inputs are all high and IOP's 1, 2, 4 are transmitted into the device selector at their appropriate times, IOT's 1, 2, 4 are then generated.

At IOT 1 time the 10 bits of data from the #1 A/D Converter (Word A) are transferred via the bus driver onto the positive bus of the PDP-8/I or PDP-8/L. From there it is handled under program control to be stored in some location in memory, or acted upon according to the program instructions.

At IOT 2 time the data on word "B" registers (#2 A/D) is transferred in the same manner onto the positive bus of the computer, and acted upon under program control.

At IOT 4 time the 12 bits from the digital clock are transferred and controlled in the same manner as were words "A" and "B".

It should be noted that words "A" and "B" are accepting only 10 bits of information; therefore, bits 11 and 12 of register A-B should be tied to ground. This is to ensure that they remain in the low (0) state and not the high (1) state.

**Sample Program**
**M734 Command Sequences — Figure 1**

Load Word A into AC
```
7200
6XY1
```

Load Word B into AC
```
7200
6XY2
```

Load Word C into AC
```
7200
6XY4
```

**Parallel Loading of 20-Bit Word into PDP-8/L — Figure 2**

Load 12 bits into AC
```
7200
6XY1
```

Load 8 remaining bits into AC
```
7200
6XY2
```

As seen in Figure 1, the M734 can be used to transfer data from three external devices. But in each case the amount of data to be transferred consists of 12 bits or less.

Figure 2 shows how a device consisting of more than 12 bits can be transferred onto the positive I/O bus of a PDP-8/I or PDP-8/L.

In Figure 2 the data to be transferred consists of 20 bits. As shown in the example, bits 0 through 11 go to input register A (Word A), bits 0 through 11; bits 12 through 19 go to input register B (Word B), bits 0 through 7.

The code selection, IOP's, and transferring of data is done in the same manner as described in Figure 2.

It should be noted that the unused input of register B and C are tied to ground.

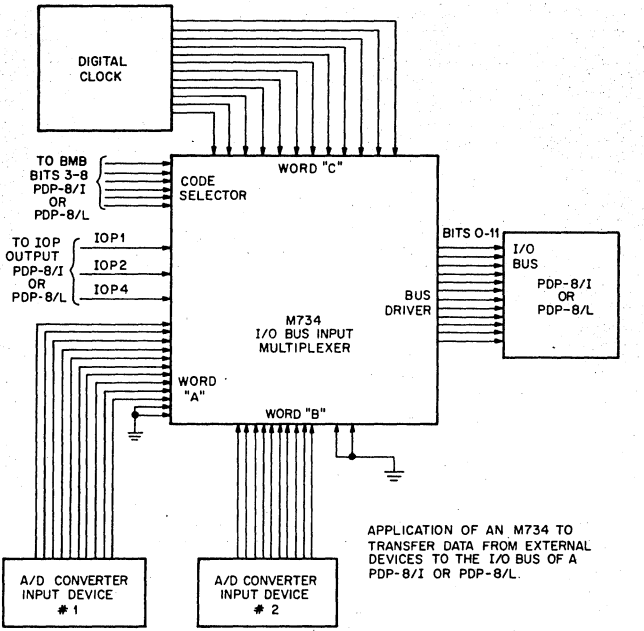



FIGURE 1. APPLICATIONS OF A M734 USED TO TRANSFER DATA FROM EXTERNAL DEVICES TO THE I/O BUS OF A PDP-8/L

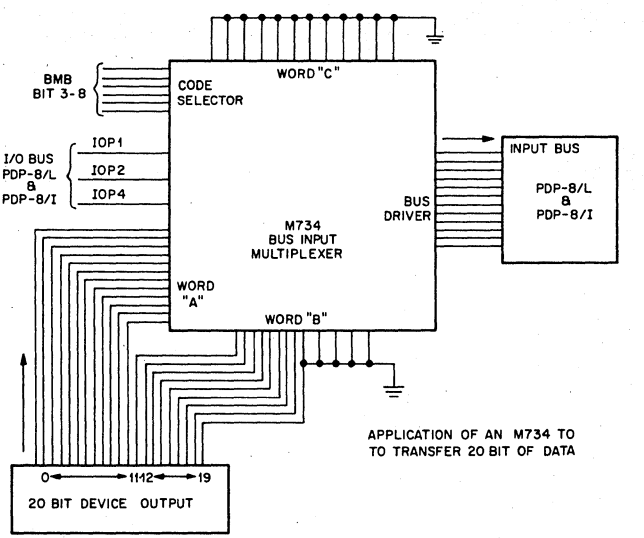



FIGURE 2. APPLICATION OF AN M734 TO TRANSFER 20 BIT OF DATA

# INTERFACING WITH PDP-8, PDP-8/I (NEGATIVE BUS)

APPLICATIONS

## 1. CABLES

For the connection of a peripheral device with M-Series logic to any PDP-8 processor with a Negative Bus or to a previous negative option, the following Y cables have to be used:

BC08C-XX — Flexprint, double sided M903 to two single sided W031's.

or BC08D-XX — Flat coaxial, double sided M904 to two single sided W011's.

The following cables have to be used between "M-Series Logic" options:

BC08A-XX — Flexprint, double sided M903 to double sided M903.

or BC08B-XX — Flat coaxial, double sided M904 to double sided M904.

## 2. GENERAL RULES FOR INTERFACING

The following rules have to be observed by designing a peripheral device with M-Series logic and positive/negative bus compatibility:

−15v has to be supplied to pin B2 of each Input/Output module.

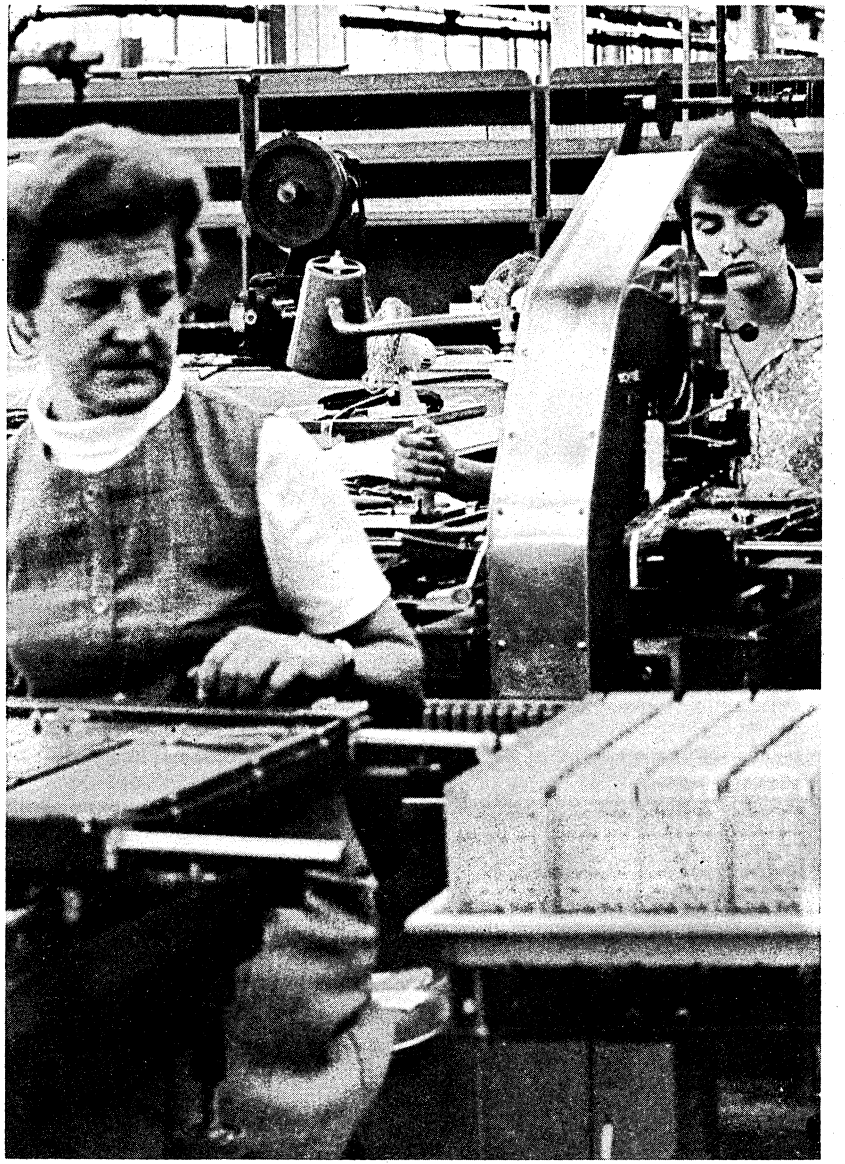
Spare gates on Input/Output modules cannot be used for any other purpose.

The two AND gates (H1, J1, K1, and L1, M1, N1) on the M102 can only be used for INITIALIZE and BTS2 or BTS3. H1 and L1 are negative inputs (assertion at −3v), J1 and M1 are TTL inputs (assertion +3v).

Do not use the inputs L2 and N2 on the M103 (restricted to the use on PDP-9 peripherals for subdevice selection).

Connect MB-bits 3 to 8, which are in assertion for the selected device, to pins D2, E2, F2, H2, J2, K2 in the appropriate connector for the M103 and M102 respectively, and connect the complements of MB-bits 3 to 8 (not in assertion) to pins P1, R1, S1, U1, M2, T2.

Never use the M100 without the Enabling Line (pin C1) connected to the Device Selector. Never use the Enabling Line as a strobe input.



Discrete components for DIGITAL Modules are positioned and crimped in place at rates up to 2,200 per hour on pantograph controlled inserting machines. Board layouts put like parts in rows, minimizing the effort required to follow the template. Several templates for each module type are generated by numerically controlled milling machines.

# EQUALITY AND RELATIVE MAGNITUDE DETECTION

APPLICATIONS

## INTRODUCTION

This application describes one method of comparing two binary numbers for equality (A = B) and relative magnitude (A > B). Figure 1 shows 2 bits of a detector using M113, M117 and M121 modules. A 4-bit section requires sixteen two input NAND gates (1 3/5 M113), five — four input NAND gates (5/6 M117), and four AND/NOR gates (2/3 M121).

Each bit of the comparator functions with two independent circuit sections; the equality detector and the magnitude detector.

## THE EQUALITY DETECTOR

Figure 2 shows just the equality detector used in each bit. The two AND gates in the AND/NOR gate actual detect $A_N \oplus B_N$ ($\oplus$ is exclusive OR) but since the output section of the AND/NOR gate also performs an inversion, the result is $\overline{A_N \oplus B_N}$ or equivalently $A_N = B_N$. This result can be verified in the truth table in Figure 3. If only equality detection is required, the output from a group of these detectors can be NANDed together with one gate of an M117 to give an "$\overline{A = B}$" signal at the output. For expansion to 16 bits, the "$\overline{A = B}$" signal from four 4-bit sections can be fed into a negative input OR gate (ie. another gate of an M113) to give an "A = B" signal from each 4 bits and then NANDed again with an M117 to provide up to 16 bit equality detection.

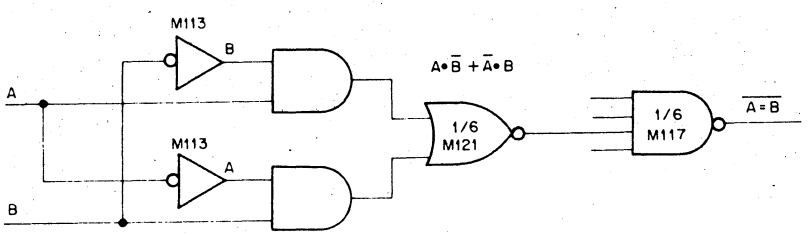



Figure 2.

| $A_N$ | $B_N$ | $A \cdot \overline{B_N}$ | $\overline{A} \cdot B_N$ | $(A_N \cdot \overline{B_N})$ A $(\overline{A_N} \cdot B_N)$ | $A_N = B_N$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

Figure 3.

NOTE: $\overline{(A_N \ B_N) + (A_N \cdot B_N)} \Leftrightarrow A_N = B_N$
ALSO: "0" = Low
"1" = High

## THE RELATIVE MAGNITUDE DETECTOR

The relative magnitude detector at bit "N"

— receives "$A_N$", "$\overline{B_N}$", and "$(A_N = B_N)$" signals from the equality section,

— receives an "Equal so far" signal from "N + 1"

— generates output signals "Equal so far" and "$\overline{A_N > B_N}$".

The input signal "Equal so far" from bit "N + 1" indicates that all bits more significant than N are equal if HIGH (ie. +3 volts). Conversely, if LOW (ground) it indicates that at least one of the more significant bits is not equal. The output "Equal so far" from bit "N" being HIGH indicates that all bits up to and including bit N are equal. A LOW indicates an inequality at or before bit N. The "$\overline{A_N > B_N}$" signal will be LOW if $A_N = 1$ and $B_N = 0$ and all more significant bits are equal. By conditioning the "$\overline{A_N > B_N}$" signal with equality information from more significant bits, it is insured that if $B_N = 1$ and $A_N = 0$, an "$\overline{A_{N-X} > B_{N-X}}$" signal cannot be enabled to give a false A > B signal at the output (bit "N-X" is simply some bit less significant than bit "N"). Thus only the most significant level of inequality is considered if two numbers are unequal. In addition to the bit schematic of Figure 4, Figure 5 shows the truth table for the relative magnitude detector part of each bit.

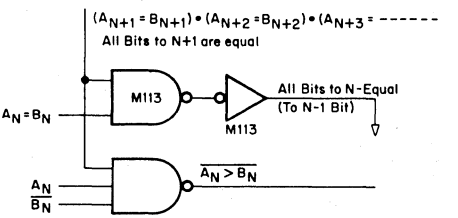



Figure 4.

| INPUTS TO BIT N | | | OUTPUTS FROM BIT N | |
|---|---|---|---|---|
| Equal to Bit N + 1 | $A_N$ | $B_N$ | "Equal to Bit N" | $A_N > B_N$ |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Figure 5.

A true XOR gate may be implemented using four-tenths of an M113, economizing by one (1) gate over the XOR in figure 3.

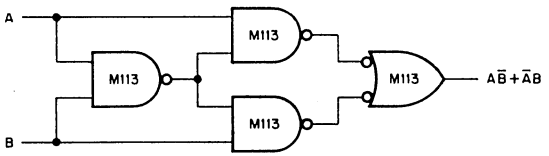



Figure 6.

## USING THE EQUALITY AND RELATIVE MAGNITUDE DETECTOR

Figure 1 shows the construction of a two bit section of the detector. There are two outputs "A > B" and "Equal to bit N-1". The "A = B" output from the detector will always come from the least significant bit regardless of the number of bits in the detector. Figure 7 summarizes the meanings of the various possible output signals.

As in the case of the equality detector, the relative magnitude detector can be expanded to 16 bits by the method shown in Figure 8. It can be expanded further to as many bits as necessary by using "A > B" outputs from 16 bit sections to feed an extender such as that in Figure 8.

Since equality information must propagate from the most significant bit to the least significant bit, the propagation delay should be considered in each application. Each bit has a 30 nanosecond delay and if the extension in Figure 8 is used there is an extra 30 nanosecond delay for the total detector. Thus a 16 bit equality and magnitude detector would have a propagation delay of (16) (30 nsec) + 30 ns = 520 nanoseconds.

## DETECTOR OUTPUT SUMMARY

| A > B | A = B (at least significant bit) | Output Indication |
|---|---|---|
| 0 (low)) | 0 (low) | B > A |
| 0 (low) | 1 (high) | A = B |
| 1 (high) | 0 (low) | A > B |
| 1 (high) | 1 (high) | impossible |

Figure 7

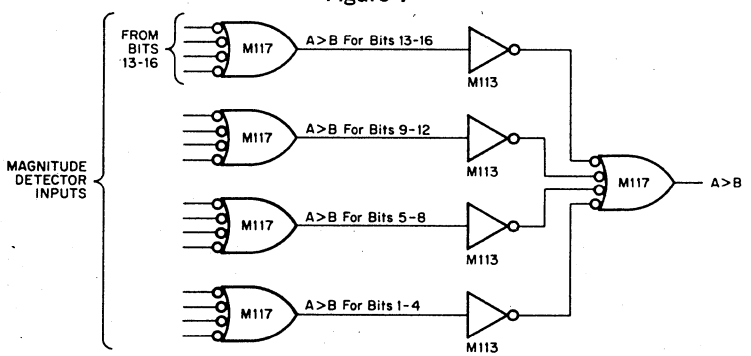



Figure 8

Table 1 gives the modules and pro-rated cost of a four bit equality detector.

Table 2 gives the modules necessary and the cost of a 4 bit equality and relative magnitude detector pro-rated according to module range. The gates required to extend the A > B output for more than four bits (see figure 8) are available as spare gates on the modules mentioned for each 4 bit section.

**TABLE 1**

| DESCRIPTION | MODULE | QUANTITY | TOTAL PRICE |
|---|---|---|---|
| 2 Input NAND gates | M113 | 4/5 | $16.00 |
| 4 Input NAND gates | M117 | 1/6 | 3.50 |
| AND/NOR gates | M121 | 2/3 | 16.60 |
| | | | $36.16 |

**TABLE 2**

| DESCRIPTION | MODULE | QUANTITY | TOTAL PRICE |
|---|---|---|---|
| 2 Input NAND gates | M113 | 1 3/5 | $32.00 |
| 4 Input NAND gates | M117 | 5/6 | 17.50 |
| AND/NOR gates | M121 | 2/3 | 16.66 |
| | | | $66.16 |

# VOLTAGE CONTROL OF THE M401 VARIABLE CLOCK

APPLICATIONS

The pulse repetition frequency of the M401 may be controlled or modulated by applying a variable voltage to the base of Q1. This may be accomplished as follows:

1. Open the connection between the base of Q1 and the junction of the resistor R1 & R2.
2. Insert a 750Ω, ±5%, ¼ watt resistor between the base of Q1 and one of the unused module terminals, F, H, L or M.
3. If the rate at which the frequency is to be changed or controlled is not excessive, add a .01 μfd. disc capacitor between the base of Q1 and ground for noise filtering.

The voltage swing applied to the resistor connected to the base of Q1 should be limited to ±0.25 volts about a center voltage of +1.5 volts. Table 1 shows the frequency excursions which one might expect when the frequency adjust potentiometer is adjusted to its full counterclockwise and full clockwise positions.

| CAPACITOR | Freq. Adj. Pot. | +1.25V | +1.50V | +1.75V |
|---|---|---|---|---|
| No Ext. Cap. | CW<br>CCW | 12.9Mhz.<br>1.02Mhz. | 13.1Mhz.<br>1.32Mhz. | 13.2Mhz.<br>1.81Mhz. |
| .001 mfd. | CW<br>CCW | 2.70Mhz.<br>72.8Khz. | 3.37Mhz.<br>97.4Khz. | 4.14Mhz.<br>142.9Khz. |
| .01 mfd. | CW<br>CCW | 382.6Khz.<br>8.19Khz. | 504.5Khz.<br>11.04Khz. | 720.4Khz.<br>16.42Khz. |
| 0.1 mfd. | CW<br>CCW | 34.46Khz.<br>722hz. | 46.54Khz.<br>972hz. | 68.93Khz.<br>1444hz. |
| 1.0 mfd. | CW<br>CCW | 3.622Khz.<br>83hz. | 5.144Khz.<br>112hz. | 8.052Khz.<br>167hz. |

# PARITY GENERATION USING THE M162

APPLICATIONS

The M162 consists of two complete parity circuits, each of which will accommodate four lines.

## 4 LINE ODD PARITY GENERATION

The following condition must exist with four line odd parity generation:

$$A \oplus B \oplus C \oplus D \Rightarrow P$$

where $\oplus$ = the modulo 2 sum.

Also, in general, the following is usually desired:

$$\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \Rightarrow P$$

or

$$(A \oplus B \oplus C \oplus D) + (\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}) \Rightarrow P$$

The M162 connected as illustrated in figure 1 will satisfy the odd parity generation as per the following truth table:

| | A | B | C | D | P |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 0 | 0 |
| 8 | 0 | 0 | 0 | 1 | 0 |
| 9 | 1 | 0 | 0 | 1 | 1 |
| | | | ↓ etc. | | |

It will be noted that the modulo 2 sum of the five bits (4 bits + parity) always yields 0 (an odd number of bits).

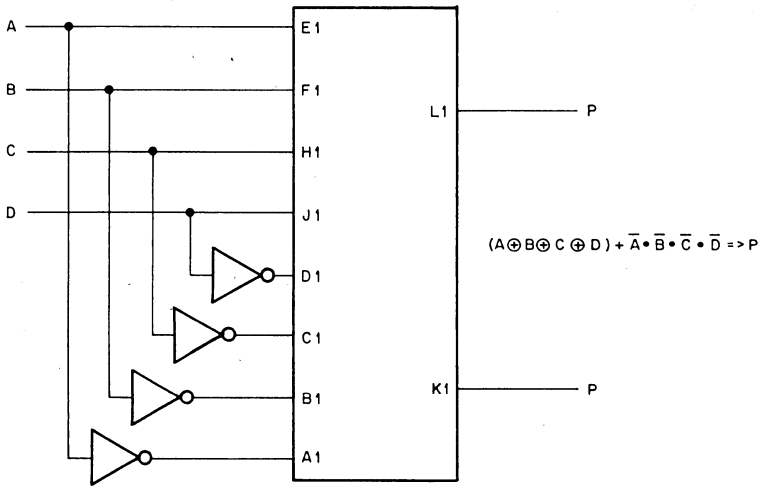



Figure 1.

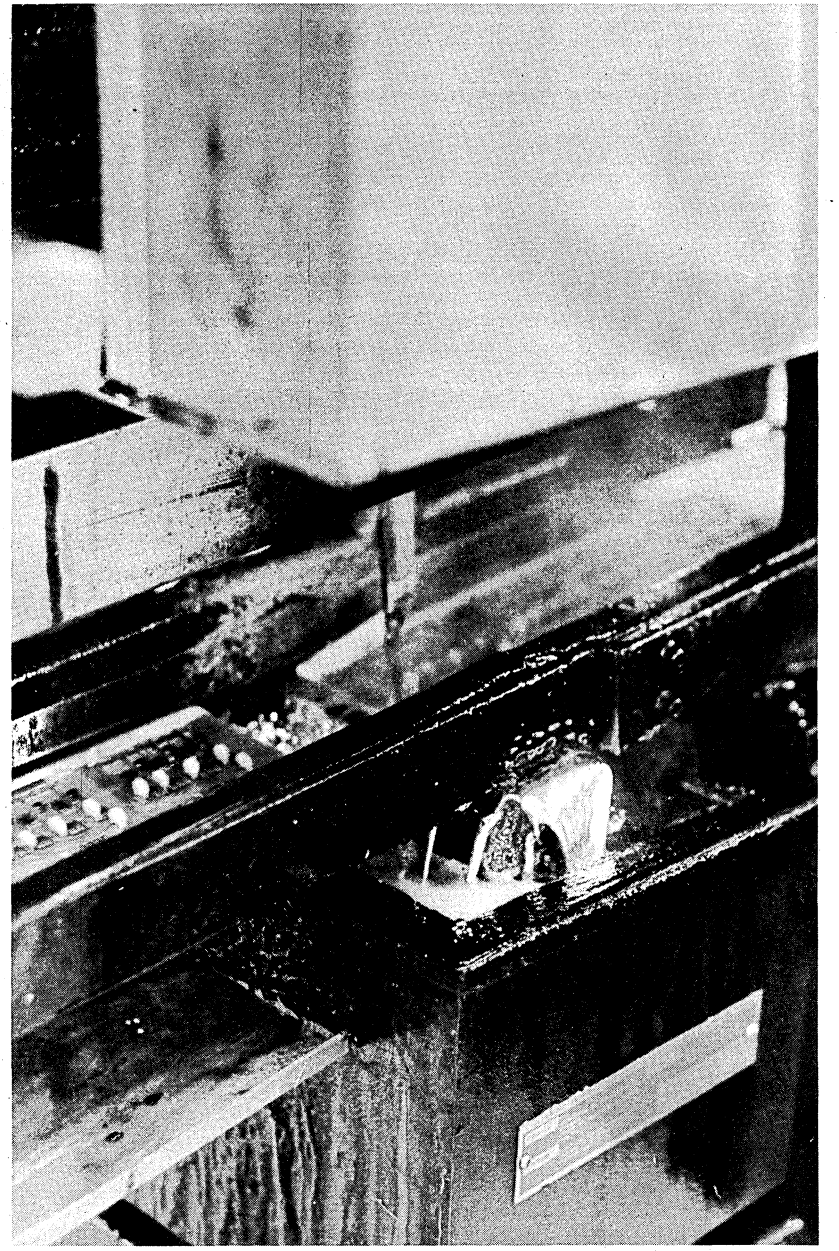
The odd parity generation with the condition $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \Rightarrow P$ will always yield an odd number of bits in the resulting character.

**7 LINE ODD PARITY GENERATION**

In this case the following would be desired:

$$(A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G) + (\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{G}) \Rightarrow P$$

This result may be obtained by connecting the M162 as shown in figure 2.



This flow-soldering machine solders all component leads to the board and makes all solder runs in one fast, exceedingly reliable, operation.

A typical device bus interface as shown in Figure 1 is composed of five major components: 1), Registers; 2), Bus Drivers and Receivers; 3), Address Selector; 4), Interrupt Control; and 5), Device Control Logic.

### Registers

Each device is assigned bus addresses at which the program can interrogate and/or load the device status, control, and data registers.

As shown in Figure 1, all information flow between the device logic and the Unibus is done through the registers. In general, registers are designed to be both loadable and readable from the bus. This allows the program to use such instructions as ADD RO, REG, or INC REG. However, registers can be "one-sided," either "read-only" or "write-only." Examples of read-only bits are the DONE and BUSY flags in the device's CSR. These bits are derived from the internal state of the device logic and are not under direct program control. Write-only registers are used when it is unnecessary to read back information. Attempting to read such a register would result in an all-zero transfer. The instructions effective with this type of register are then limited to those which load the register such as MOV RO, REG, or CLR REG (as opposed to ADD REG, RO, or INC REG).

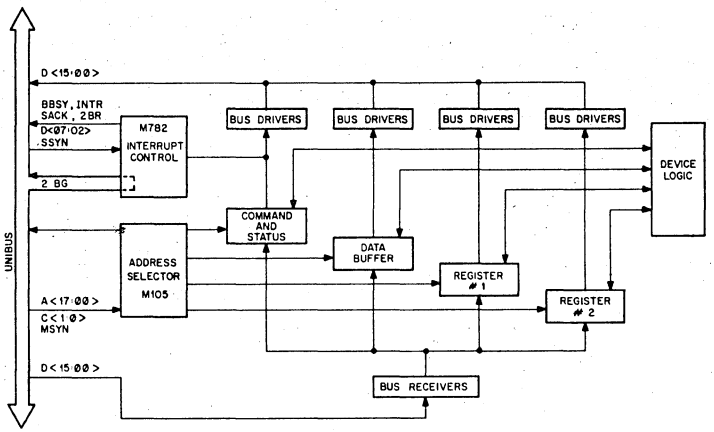
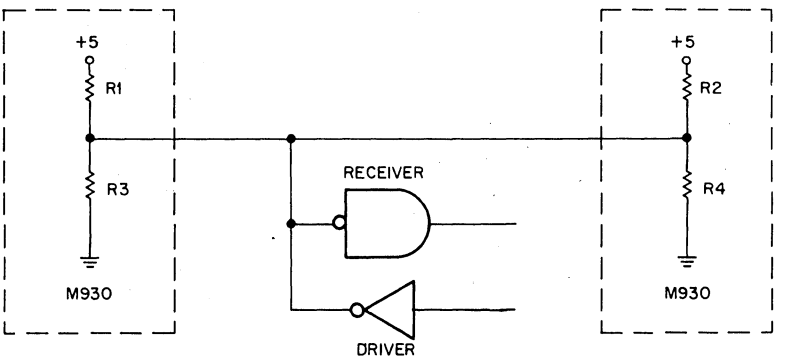



Figure 1. Typical Peripheral Device Interface

### Bus Drivers and Receivers

To maintain the transmission-line characteristics of the Unibus, special circuits are required to pass signals to and from the bus. The majority of bus signals (all except the five grant lines) are received, driven and terminated as shown in Figure 2.




R1, R2 = 180Ω 5% 1/4W
R3, R4 = 390Ω 5% 1/4W

Figure 2. Typical Unibus Line

Information is received from the bus using gates which have a high input impedance and proper logic thresholds. High input levels must be greater than 2.5 V with an input current less than 160 μa. Low level input must be less than 1.4 V with an input current greater than 0 μa.

Information transmitted on the bus must be driven with open collector drivers capable of sinking 50 ma with a collector voltage of less than .8 V. Output leakage current must be less than 25 μa.

In PDP-11 systems, the bus signals are terminated at both ends by resistor dividers provided on the M930 module. Physically, an M930 is located in the processor; another is located at the last unit on the bus. A bus signal sits at logical "0" (inactive, or negated state) at a voltage of 3.4 V. A bus line is at logical "1" (active, or asserted) when it is pulled to ground.

Drivers and receivers meeting these specifications are available on the M783, M784 and M785 modules as shown in Figures 3, 4 and 5.

### M105 Address Selector

The M105 Address Selector as shown in Figure 6 is used to provide gating signals for up to four device registers. The selector decodes the 18-bit bus address on A <17:00> as follows:

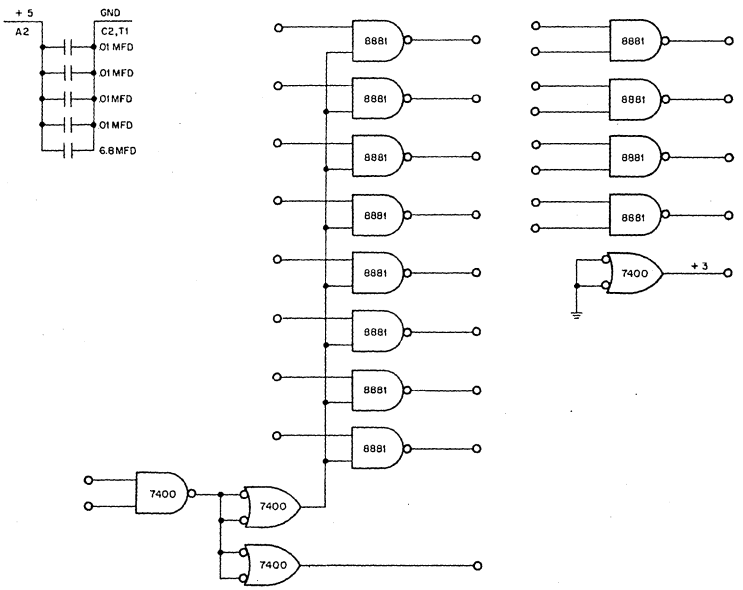



Figure 3 M783 Unibus Drivers*

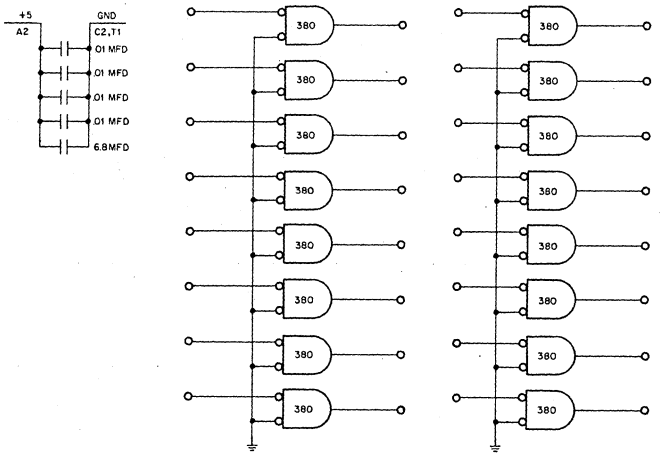



Figure 4 M784 Unibus Receivers*

*Complete technical specifications and pin assignments will be available April 15, 1970.

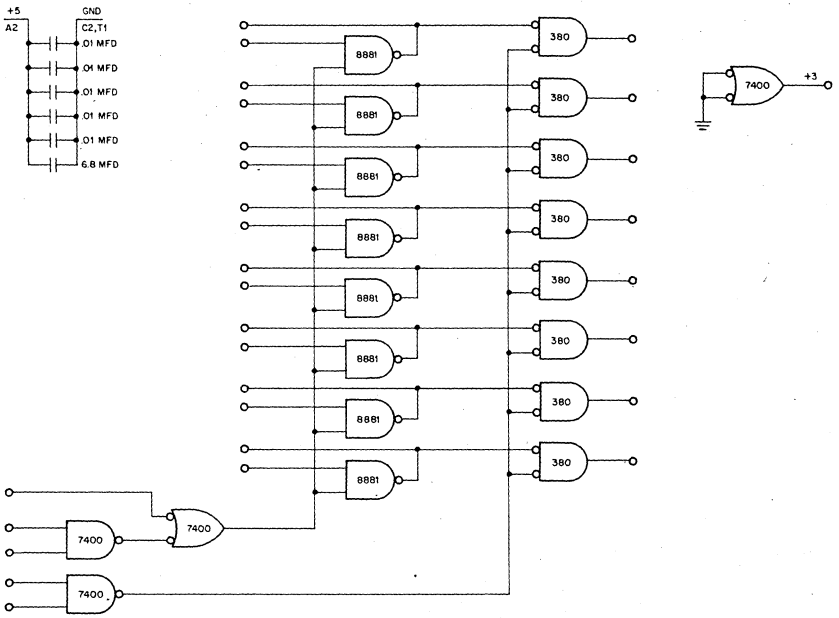



Figure 5 M785 Unibus Drivers and Receivers*

A00 is used for byte control. A01 and A02 are decoded to provide one of four addresses. A <12:03> are determined by jumpers on the card. When the jumper is in, the selector will look for a 0 on that address line-A <17:13> must all be 1's—(this defines the external bank). Other bus inputs to the selector are C <1:0> and MSYN. The single bus output is SSYN.The user signals are SELECT 0, 2, 4, and 6 (corresponding to the decoding of A02 and A01, one of which is asserted when A <17:13> are all 1's and A <12:03> compare with the state of the jumpers. Other user signals are OUT HIGH (gate data into high byte), OUT LOW (gate data into low byte), and IN (gate data onto the bus). The equations for these last three signals are as follows:

$$\begin{aligned} \text{OUT HIGH} &= \text{DATO} + \text{DATOB}*\overline{\text{A00}} \\ \text{OUT LOW} &= \text{DATO} + \text{DATOB}*\overline{\text{A00}} \\ \text{IN} &= \text{DATI} + \text{DATIP} \end{aligned}$$

where "+" means a logical or and "*" means a logical and.

Use of the M105, drivers, receivers and a flip-flop register is shown in Figure 7.

*Complete technical specifications and pin assignments will be available April 15, 1970.

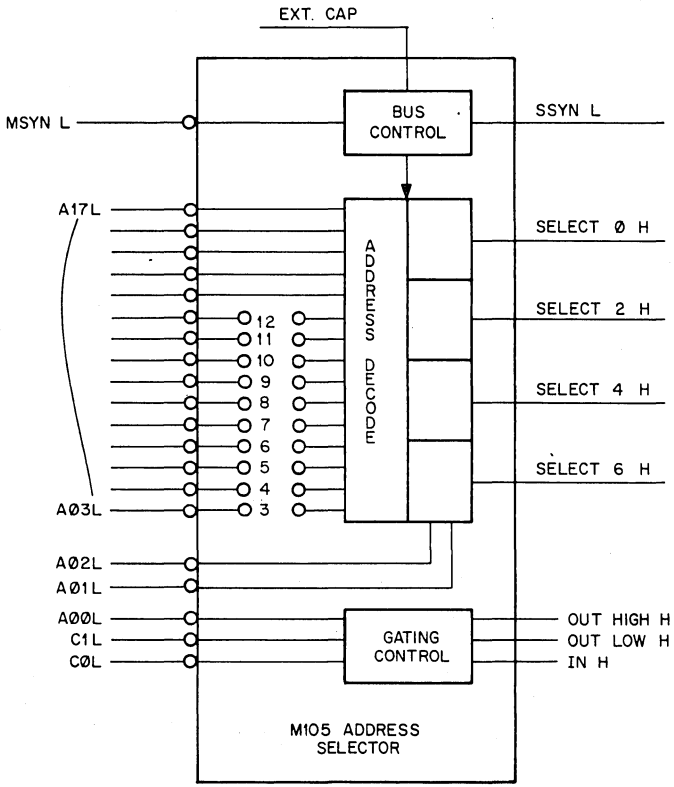



Figure 6 M105 Address Selector

**M782 Interrupt Control***

The M782 Interrupt Control module contains the necessary logic circuits to allow a peripheral device to gain bus control and perform a program interrupt. The three circuits on this card are block diagrammed in Figure 8. Note that only signals relevant to the user's interface are shown; bus signals SSYN, BBSY and SACK have been omitted for clarity.

The Master Control circuit is used to gain bus control. When INT and INT ENB are asserted, a bus request is made on the request line to which BR is jumpered. When the processor issues the correponding grant and other bus conditions are met, the MASTER signal is asserted, indicating that this device now has bus control. Note that this circuit also can be used to gain bus control on an NPR line for a device which requests the bus for direct memory access.

*Complete technical specifications and pin assignments will be available April 15, 1970.

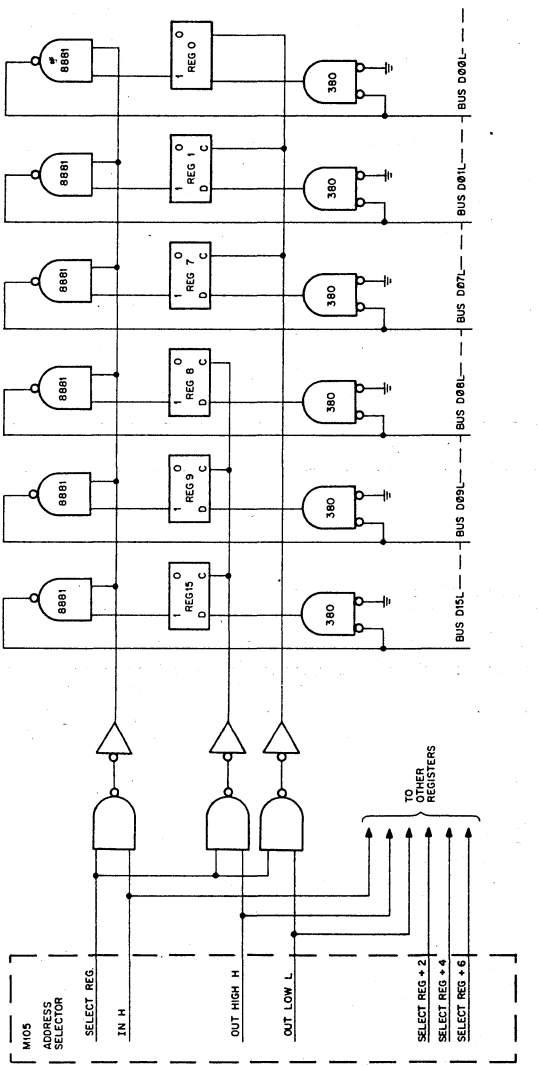



Figure 7 Typical Peripheral Device Register

In addition to two Master Control circuits, a third logic network provides the necessary signals and gating to perform the INTR bus operation. When either of the START INTR signals is asserted, the INTR bus signal is asserted along with a vector address on D <07:02>. Bits 07:03 are determined by jumpers on the card. A jumper "in" forces a 0 in that bit. Bit 2 is controlled by Vector Bit 2. When the processor responds to the INTR signal by asserting SSYN, the INTR DONE signal is asserted. This line is used to clear the condition which asserted INTR START.

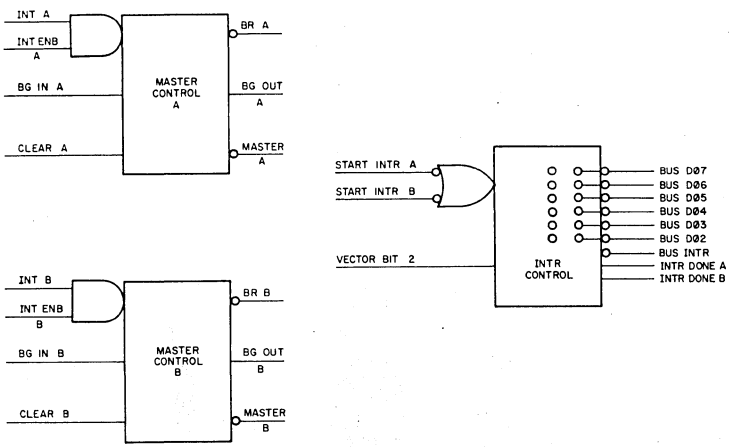



Figure 8 M782 Interrupt Control

Figure 9 shows a possible interconnection of the M782 to provide independent interrupts for two possible conditions in a device: ERROR and DONE. The ERROR and DONE signals shown in Figure 9 are signals from bits 15 and 7 in a device's CSR. Likewise ERROR INT ENB and DONE INT ENB are derived from the CSR. Both interrupts in this example are tied to the BR4 level; the corresponding grant line BG4 enters the ERROR Master Control and is passed on to the DONE Master Control. Thus, ERROR has a slightly higher priority interrupt level than DONE.

Both MASTER signals are tied to the INTR control. Thus, whenever either ERROR or DONE gains bus control, an INTR operation is initiated. Note that Vector Bit 2 is a 1 or 0 as a function of which master control is interrupting. Also, INTR DONE is tied to MASTER CLEAR to clear the master condition.

## Device Control Logic

The type of control logic for a peripheral depends on the nature of the device. Digital offers a wide line of general-purpose logic modules for implementing control logic.

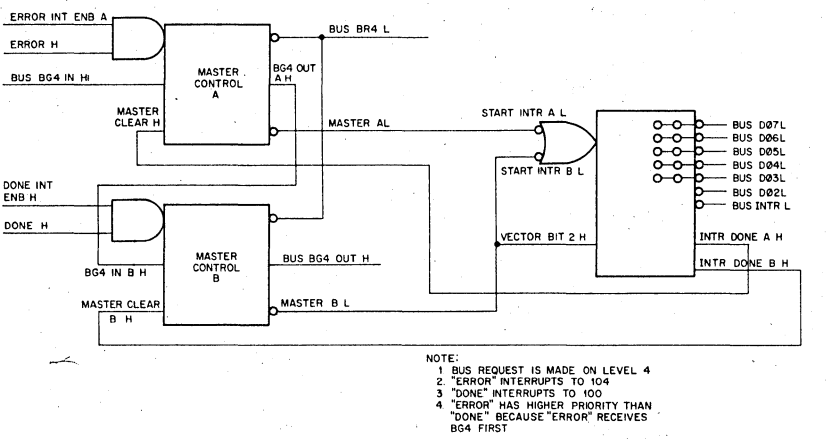



Figure 9. Typical Interconnection of M782 Interrupt Control

**Modular Construction**

Physically, the PDP-11 is composed of a number of System Units. Each System Unit is composed of three 8-slot connector blocks mounted end-to-end as shown in Figure 1. The Unibus connects to the System Unit at the lower left and at the upper left. Power also connects to the unit in the leftmost back. A System Unit is connected to other System Units only via the Unibus.

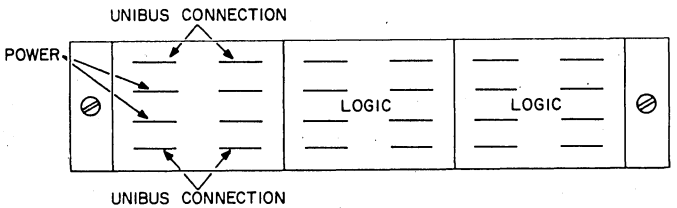



Figure 1 System Unit

The remainder of the System Unit contains logic for the processor, memory or an I/O device interface. This logic is composed of single height, double height, or quad height modules which are 8.5" deep.

The use of System Units allows the PDP-11 to be optimally packaged for each individual application. Up to six System Units can be mounted into a single mounting box. For a basic PDP-11/20 system, the processor/console would fill 2½ System Unit spaces and 4096 words of core memory would fill one System Unit space. This leaves 2½ spaces for user-designated options. This would allow the user to add 8,192 words of additional core memory, a Teletype control, and a High-Speed Paper Tape Control, or 4,096 words of core memory and six Teletype interfaces. Larger systems will require a BA11-EC or BA11-ES Extension Mounting Box which contains space for six additional System Units.

The use of System Units also facilitates expansion of systems in the field and service. To add an additional option to a PDP-11 system, the proper System Unit is mounted in the Basic or Extension Mounting Box and the Unibus is extended. Servicing of the PDP-11 can be done by swapping modules or by swapping System Units.

**Blank System Unit (BB11)**—The BB11 consists of three 288-pin connector blocks connected end-to-end. This unit is unwired except for Unibus and power connections and allows customer-built interfaces to be integrated easily into a PDP-11 system. For mounting it requires one-sixth (1/6) of a BA11 Mounting Box.

**Unibus Module (M920)**—The M920 is a double module which connects the Unibus from one System Unit to the next within a Mounting Box. The printed circuit cards are separated by 1″ for this purpose. A single M920 will carry all 56 Unibus signals and 14 grounds.

**Unibus Cable (BC11A)**—The BC11A is a 120-conductor flexprint cable used to connect System Units in different mounting boxes or a peripheral device which is removed from the mounting boxes.

The 120 signals consist of the 56 Unibus lines plus 64 grounds. Signals and grounds alternate to minimize cross talk.

| Type | Length |
|---|---|
| BC11A-2 | 2′ |
| BC11A-5 | 5′ |
| BC11A-8A | 8′6″ |
| BC11A-10 | 10′ |
| BC11A-15 | 15′ |
| BC11A-25 | 25′ |

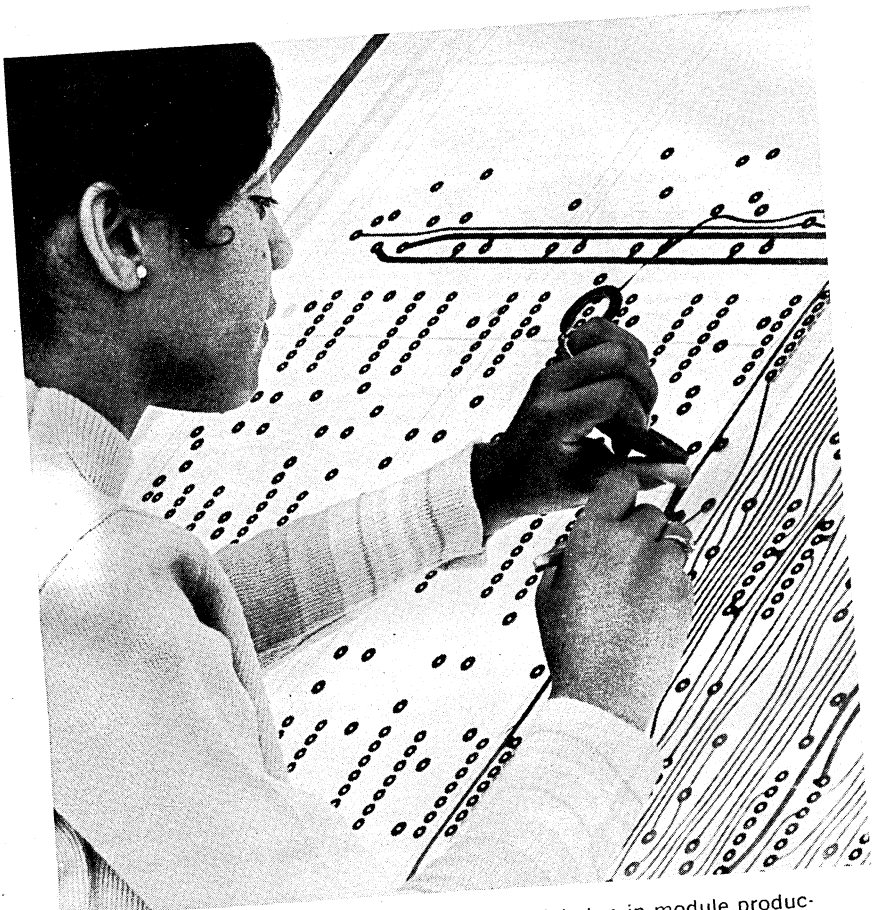
**Cable Requirements**

When an Extension Mounting Box is used, an external cable, the BC11A, is the only signal connection between mounting boxes. This external bus cable may also be used to connect other peripherals to the PDP-11. The maximum combined, internal and external, bus cable length is 50′.

## PDP-11 INTERFACING MODULES

### Price Summary

| TYPE NUMBER | DESCRIPTION | PRICE |
|---|---|---|
| BB11 | Blank Mounting Panel — Wired for bus and power<br>(Does not include UNIBUS connector Module — M920)<br>For custom interface design and mounting | $ 90 |
| M783 | UNIBUS Transmitter Module<br>UNIBUS to Device interface drivers (12) drivers | $ 30 |
| M784 | UNIBUS Receiver Module<br>UNIBUS to Device interface receivers (16) receivers | $ 30 |
| M785 | UNIBUS Transceiver Module<br>UNIBUS/Device interface drivers and receivers<br>(8) receivers and (8) drivers | $ 35 |
| M105 | Address Selector Module (4 Addresses) | $ 65 |
| M782 | Interrupt Control Module (2 interrupt capability) | $100 |
| M920 | UNIBUS Connector Module<br>(Jumper module to interconnect System Units) | $ 45 |
| BC11A | UNIBUS Cable Length | |
| | BC11A-2 2′ | $ 80 |
| | BC11A-5 5′ | $ 90 |
| | BC11A-8A 8′6″ | $100 |
| | BC11A-10 10′ | $110 |
| | BC11A-15 15′ | $125 |
| | BC11A-25 25′ | $160 |



The printed circuit board layout is a crucial step in module production. Tolerances are checked to within 1/5000 of an inch.

# PRICE LIST AND NUMERICAL INDEX

| | PRICES EFFECTIVE MARCH 23, 1970 | Price | Page |
|---|---|---|---|
| A123 | Positive Logic Multiplexer | $ 58.00 | 228 |
| A200 | Operational Amplifier | 130.00 | 230 |
| A206 | Operational Amplifier | 190.00 | 232 |
| A207 | Operational Amplifier | 45.00 | 234 |
| A404 | Sample and Hold | 130.00 | 235 |
| A613 | 12-Bit DAC | 250.00 | 238 |
| A618 | 10-Bit D/A Converter Single Buffered | 350.00 | 240 |
| A619 | 10-Bit D/A Converter Single Buffered | 375.00 | 240 |
| A620 | 10-Bit D/A Converter Double Buffered | 400.00 | 242 |
| A621 | 10-Bit D/A Converter Double Buffered | 425.00 | 242 |
| A702 | Reference Supply | 58.00 | 244 |
| A704 | Reference Supply | 184.00 | 244 |
| A811 | 10-Bit A/D Converter | 450.00 | 246 |
| A990 | Amplifier Boards | 4.00 | 248 |
| A992 | Amplifier Boards | 4.00 | 248 |
| B104 | Inverter | 17.00 | 253 |
| B105 | Inverter | 21.00 | 253 |
| B113 | NAND/NOR Gate | 23.00 | 253 |
| B115 | NAND/NOR Gate | 21.00 | 253 |
| B117 | NAND/NOR Gate | 14.00 | 253 |
| B123 | Inverter | 31.00 | 253 |
| B124 | Inverter | 31.00 | 253 |
| B130 | Three-Bit Parity Circuit | 50.00 | 254 |
| B155 | Half Binary to Octal Decoder | 25.00 | 254 |
| B171 | NAND/NOR Gate | 18.00 | 253 |
| B200 | Flip-Flop | 25.00 | 255 |
| B201 | Flip-Flop | 56.00 | 255 |
| B204 | Quadruple Flip-Flop | 29.00 | 255 |
| B301 | Delay (One Shot) | 73.00 | 256 |
| B310 | Delay | 66.00 | 256 |
| B360 | Delay with Pulse Amplifier | 84.00 | 257 |
| B401 | Clock (Varible) | 57.00 | 257 |
| B405 | Clock (Crystal) | 100.00 | 257 |
| B602 | Pulse Amplifier | 36.00 | 258 |
| B620 | Carry Pulse Amplifier | 47.00 | 258 |
| B681 | Power Inverter | 25.00 | 259 |
| B684 | Bus Driver | 52.00 | 259 |
| BB11 | Blank Mounting Panel | 90.00 | 425 |
| BC11A-2 | UNIBUS Cable (2′ length) | 80.00 | 425 |
| BC11A-5 | UNIBUS Cable (5′ length) | 90.00 | 425 |
| BC11A-8A | UNIBUS Cable (8′ 6″ length) | 100.00 | 425 |
| BC11A-10 | UNIBUS Cable (10′ length) | 110.00 | 425 |
| BC11A-15 | UNIBUS Cable (15′ length) | 125.00 | 425 |
| BC11A-25 | UNIBUS Cable (25′ length) | 160.00 | 425 |
| H001 | Bracket | 8.00 | 312 |
| H002 | Bracket | 8.00 | 312 |
| H020 | Frame Casting | 15.00 | 312 |
| H021 | End Plates | 7.00 | 312 |
| H022 | End Plate Assembly | 20.00 | 312 |

| | | Price | Page |
|---|---|---|---|
| H701 | Power Supply | $116.00 | 297 |
| H701A | Power Supply | 136.00 | 297 |
| H704 | Dual Power Supply | 200.00 | 299 |
| H707 | Dual Power Supply | 400.00 | 299 |
| H710 | Power Supply | 200.00 | 301 |
| H716 | Power Supply | 150.00 | 302 |
| H800 | Connector Block | 150.00 | 307 |
| H801 | Replacement Contacts | 2.00 | 307 |
| H802 | Connector Block | 4.00 | 308 |
| H803 | Connector Block | 13.00 | 309 |
| H805 | Replacement Contacts | 4.00 | 309 |
| H807 | Connector Blocks | 5.00 | 310 |
| H808 | Connector Blocks | 10.00 | 311 |
| H809 | Replacement Contacts | 4.00 | 311 |
| H810 | Pistol Grip Wire-Wrapping Tool | 99.00 | 337 |
| H811 | Hand Wrapping Tool | 21.50 | 337 |
| H812 | Hand Unwrapping Tool | 10.50 | 337 |
| H813 | Hand Unwrapping Tool | 30.00 | 337 |
| H814 | Hand Unwrapping Tool | 21.00 | 337 |
| H820 | Grip Clip | 48.00 | 334 |
| H821 | Grip Clip | 75.00 | 334 |
| H825 | Hand Crimping Tool | 146.00 | 334 |
| H826 | Hand Crimping Tool | 210.00 | 334 |
| H910 | Mounting Panel | 280.00 | 315 |
| H911J | Mounting Panel | 151.00 | 317 |
| H913 | Mounting Panel | 270.00 | 318 |
| H914 | Mounting Panel | 125.00 | 318 |
| H916 | Mounting Panel | 270.00 | 318 |
| H917 | Mounting Panel | 260.00 | 318 |
| H920 | Module Drawer | 170.00 | 321 |
| H925 | Module Drawer | 250.00 | 322 |
| H941-AA | Mounting Panel 19" | 175.00 | 323 |
| H950-AA | Cabinet | 152.00 | 326 |
| K003 | Gate Expander | 5.00 | 168 |
| K012 | Gate Expander | 8.00 | 168 |
| K026 | Gate Expander | 8.00 | 168 |
| K028 | Gate Expander | 8.00 | 168 |
| K080 | Cable Connector | 3.00 | 176 |
| K113 | Logic Gate | 11.00 | 168 |
| K123 | Logic Gate | 12.00 | 168 |
| K124 | Logic Gate | 14.00 | 168 |
| K134 | Inverter | 13.00 | 169 |
| K135 | Inverter | 13.00 | 169 |
| K161 | Binary to Octal Decoder | 25.00 | 169 |
| K174 | Digital Comparator | 24.00 | 169 |
| K184 | Rate Multiplier | 25.00 | 169 |
| K201 | Flip-Flop | 39.00 | 169, 177 |
| K202 | Flip-Flop | 27.00 | 169 |
| K206 | Flip-Flop Register | 20.00 | 169 |
| K210 | Counter | 27.00 | 170 |
| K211 | Programmable Divider | 20.00 | 170 |
| K220 | Up/Down Counter | 55.00 | 170 |

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|---|---|---|---|
| K230 | Shift Register | $ 40.00 | 170 |
| K271 | Retentive Memory | 40.00 | 170 |
| K273 | Retentive Memory | 85.00 | 170 |
| K281 | Fixed Memory | 10.00 | 170 |
| K301 | Basic Timer | 15.00 | 170 |
| K303 | Timer | 27.00 | 170 |
| K323 | One Shot | 35.00 | 170 |
| K333 | Pulser | 23.00 | 170, 178 |
| K371 | Timer Control, Clock | 11.00 | 170 |
| K373 | Timer Control, Clock | 11.00 | 170 |
| K374 | Calibrated Timer Control | 15.00 | 170 |
| K375 | Timer Control Clock | 11.00 | 170 |
| K376 | Calibrated Timer Control | 15.00 | 170 |
| K378 | Calibrated Timer Control | 15.00 | 170 |
| K410 | Indicator Lights | 18.00 | 171, 185 |
| K420 | Switches | 33.00 | 171, 185 |
| K422 | Thumbwheel Encoder | 27.00 | 171 |
| K424 | Thumbwheel Decoder | 27.00 | 171 |
| K432 | Timer Control | 33.00 | 171, 187 |
| K501 | Schmitt Trigger | 25.00 | 172 |
| K508 | AC Input Converter | 44.00 | 172 |
| K522 | Sensor Converter | 25.00 | 172 |
| K524 | Sensor Converter | 98.00 | 172 |
| K531 | Quadrature Decoder | 70.00 | 172 |
| K578 | 120 VAC Input Converter | 80.00 | 172, 200 |
| K580 | Dry Contact Filter | 28.00 | 172, 202 |
| K581 | Dry Contact Filter | 20.00 | 172, 202 |
| K596 | EIA Input Converter | 20.00 | 172, 205 |
| K604 | Isolated AC Switch | 110.00 | 172, 206 |
| K614 | Isolated AC Switch | 88.00 | 172, 208 |
| K615 | Isolated AC Switch | 92.00 | 172, 180 |
| H644 | DC Driver | 66.00 | 172, 209 |
| K656 | DC Driver | 80.00 | 172, 211 |
| K658 | DC Driver | 128.00 | 172, 212 |
| K671 | Decimal Decoder & Nixi Display | 55.00 | 172, 213 |
| K681 | Lamp Driver | 15.00 | 172, 214 |
| K683 | Lamp Driver | 30.00 | 172, 214 |
| K696 | EIA Output Converter | 44.00 | 172, 216 |
| K716 | Interface Block | 75.00 | 173 |
| K724 | Interface Shell | 55.00 | 173 |
| K730 | Source and Control Module | 19.00 | 174, 182 |
| K731 | Source Module | 30.00 | 174, 303 |
| K732 | Slave Regulator | 27.00 | 174, 303 |
| K741 | Power Transformer | 30.00 | 174, 304 |
| K743 | Power Transformer | 45.00 | 174, 304 |
| K771 | Display Supply | 35.00 | 174, 306 |
| K782 | Terminal | 12.00 | 174 |
| K784 | Terminal | 17.00 | 174 |
| K791 | Test Probe | 40.00 | 174 |
| K900 | Control Panel-Power Supply | 185.00 | 352 |
| K901 | Patch Board Panel | 125.00 | 353 |
| K902 | Indicator Switch Panel | 145.00 | 354 |

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|---|---|---|---|
| K940 | Mounting Hardware | $ 4.00 | 175 |
| K941 | Mounting Hardware | 6.00 | 175 |
| K943 | Mounting Panel | 96.00 | 175 |
| K950 | Modular Mounting Hardware | 39.00 | 175, 217 |
| K980 | End Plates | 6.00 | 175 |
| K982 | Mounting Panel | 10.00 | 175, 184 |
| K990 | Timer Component Board | 4.00 | 175 |
| M002 | Logic 1 Source | 10.00 | 21 |
| M040 | Solenoid Driver | 39.00 | 22 |
| M050 | 50ma Indicator Driver | 31.00 | 24 |
| M051 | Lever Converter | 31.00 | 25 |
| M100 | Bus Data Interface | 50.00 | 26 |
| M101 | Bus Data Interface | 24.00 | 28 |
| M102 | Device Selector | 60.00 | 30 |
| M103 | Device Selector | 45.00 | 32 |
| M105 | Address Selector Module | 45.00 | 45 |
| M107 | Device Selector | 105.00 | 34 |
| M108 | Flag Module | 45.00 | 38 |
| M111 | Inverter | 22.00 | 40 |
| M112 | NOR Gate | 35.00 | 41 |
| M113 | Ten 2-Input NAND Gates | 18.00 | 42 |
| M115 | Eight 3-Input NAND Gates | 18.00 | 42 |
| M117 | Six 4-Input NAND Gates | 19.00 | 42 |
| M119 | Three 8-Input NAND Gates | 18.00 | 42 |
| M121 | AND/NOR Gate | 23.00 | 45 |
| M133 | Input NAND Gates | 27.00 | 46 |
| M141 | NAND/OR GATES | 29.00 | 47 |
| M160 | AND/NOR Gate | 33.00 | 49 |
| M161 | Binary to Octal/Decimal Decoder | 55.00 | 50 |
| M162 | Parity Circuit | 63.00 | 52 |
| M169 | Gating Module | 33.00 | 53 |
| M202 | Triple J-K Flip-Flop | 29.00 | 54 |
| M203 | 8 R/S Flip-Flop | 26.00 | 56 |
| M204 | General Purpose Buffer and Counter | 34.00 | 58 |
| M206 | General Purpose Flip-Flop | 30.00 | 60 |
| M207 | General Purpose Flip-Flop | 33.00 | 62 |
| M208 | 8-Bit Buffer/Shift Register | 80.00 | 64 |
| M211 | Binary Up/Down Counter | 69.00 | 67 |
| M213 | BCD Up/Down Counter | 86.00 | 68 |
| M302 | Dual Delay Multivibrator | 50.00 | 72 |
| M306 | Integrating One Shot | 27.00 | 74 |
| M310 | Delay Line | 58.00 | 76 |
| M360 | Variable Delay | 68.00 | 77 |
| M401 | Variable Clock | 55.00 | 78 |
| M405 | Crystal Clock | 100.00 | 80 |
| M410 | Reed Clock | 70.00 | 82 |
| M452 | Variable Clock | 40.00 | 84 |
| M500 | Negative Input Positive Output Receiver | 55.00 | 85 |
| M501 | Schmitt Trigger | 25.00 | 86 |
| M502 | Negative Input Converter | 26.00 | 88 |
| M506 | Negative Input Converter | 52.00 | 89 |
| M507 | Bus Converter | 45.00 | 90 |

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|---|---|---|---|
| M510 | I/O Bus Receiver | $51.00 | 92 |
| M602 | Pulse Amplifier | 28.00 | 94 |
| M606 | Pulse Generator | 43.00 | 96 |
| M617 | Four Input Power NAND Gate | 26.00 | 98 |
| M622 | Eight Bit Positive Input/Output Bus Driver | 45.00 | 100 |
| M623 | Bus Driver | 40.00 | 102 |
| M624 | Bus Driver | 45.00 | 104 |
| M627 | NAND Power Amplifier | 29.00 | 106 |
| M632 | Positive Input Negative Output Bus Driver | 55.00 | 108 |
| M633 | Negative Bus Driver | 50.00 | 110 |
| M650 | Negative Output Converter | 25.00 | 112 |
| M652 | Negative Output Converter | 26.00 | 113 |
| M660 | Positive Level Driver | 25.00 | 114 |
| M661 | Positive Level Driver | 15.00 | 115 |
| M706 | Teletype Receiver | 150.00 | 116 |
| M707 | Teletype Transmitter | 150.00 | 121 |
| M730 | Bus Interface | 160.00 | 126 |
| M731 | Bus Interface | 160.00 | 126 |
| M732 | Bus Interface | 160.00 | 130 |
| M733 | Bus Interface | 165.00 | 130 |
| M734 | I/O Bus Input Multiplexer | 105.00 | 134 |
| M735 | I/O Bus Transfer Register | 135.00 | 136 |
| M736 | Priority Interrupt Module | 125.00 | 139, 140 |
| M737 | 12-Bit Bus Receiver Interface | 120.00 | 144 |
| M738 | Counter-Buffer Interface | 105.00 | 146 |
| M782 | Interrupt Control Module | 100.00 | 425 |
| M783 | UNIBUS Transmitter Module | 30.00 | 425 |
| M784 | UNIBUS Receiver Module | 30.00 | 425 |
| M785 | UNIBUS Transceiver Module | 35.00 | 425 |
| M901 | Flexprint Cable Connector | 15.00 | 152 |
| M903 | Flexprint Connector | 12.00 | 153 |
| M904 | Coaxial Cable Connector | 14.00 | 154 |
| M906 | Cable Terminator | 20.00 | 155 |
| M907 | Diode Clamp Connector | 16.00 | 156 |
| M908 | Ribbon Connector | 18.00 | 157 |
| M909 | Termination Card | 14.00 | 158 |
| M910 | Pull Up Resistor | 20.00 | 159 |
| M920 | UNIBUS Connector Module | 45.00 | 425 |
| R001 | Diode Network | 4.00 | 263 |
| R002 | Diode Network | 5.00 | 263 |
| R107 | Inverter | 24.00 | 263 |
| R111 | Expandable NAND/NOR Gate | 14.00 | 264 |
| R113 | NAND/NOR Gate | 20.00 | 264 |
| R121 | NAND/NOR Gate | 17.00 | 264 |
| R122 | NAND/NOR Gate | 26.00 | 265 |
| R123 | Input Bus | 19.00 | 265 |
| R131 | Exclusive OR | 35.00 | 265 |
| R141 | AND/NOR Gate | 13.00 | 266 |
| R151 | Binary-to-Octal Decoder | 33.00 | 266 |
| R181 | DC Carry Chain | 35.00 | 266 |
| R200 | Flip-Flop | 9.50 | 267 |
| R201 | Flip-Flop | 22.00 | 267 |

| | | Price | Page |
|---|---|---|---|
| R202 | Dual Flip-Flop | $25.00 | 267 |
| R203 | Triple Flip-Flop | 28.00 | 268 |
| R204 | Quadruple Flip-Flop | 28.00 | 268 |
| R205 | Dual Flip-Flop | 29.00 | 268 |
| R302 | Dual Delay Multivibrator | 44.00 | 269 |
| R303 | Integrating One Shot | 45.00 | 269 |
| R401 | Variable Clock | 45.00 | 270 |
| R405 | Crystal Clock | 100.00 | 270 |
| R601 | Pulse Amplifier | 25.00 | 270 |
| R602 | Pulse Amplifier | 22.00 | 271 |
| R603 | Pulse Amplifier | 28.00 | 271 |
| R650 | Bus Driver | 23.00 | 271 |
| W002 | Clamp Loads | 13.00 | 275 |
| W005 | Clamp Loads | 15.00 | 275 |
| W018 | Cable Connector | 9.00 | 275, 346 |
| W021 | Cable Connector | 4.00 | 346 |
| W022 | Cable Connector | 5.00 | 346 |
| W023 | Cable Connector | 4.00 | 375 |
| W028 | Cable Connector | 5.00 | 346 |
| W040 | Solenoid Driver | 36.00 | 276 |
| W042 | 10 AMP Driver | 80.00 | 276 |
| W043 | Solenoid Driver | 35.00 | 276 |
| W050 | 30 MA Indicator Driver | 13.00 | 277 |
| W051 | 100 MA Indicator and Relay Driver | 22.00 | 277 |
| W061 | Relay Driver | 35.00 | 277 |
| W080 | Isolated AC-DC Switch | 60.00 | 278 |
| W103 | PDP-8 Device Selector | 52.00 | 278 |
| W108 | Decoding Driver | 75.00 | 278 |
| W500 | High Impedance Follower | 25.00 | 279 |
| W501 | Negative Input Converter and Schmitt Trigger | 13.00 | 279 |
| W510 | Positive Input Converter | 17.00 | 280 |
| W511 | Negative Input Converter | 17.00 | 280 |
| W512 | Positive Level Converter | 25.00 | 160, 280 |
| W520 | Comparator | 43.00 | 281 |
| W532 | Dual AC Coupled Difference Amplifier | 30.00 | 281 |
| W533 | Dual Rectifying Slicer | 30.00 | 282 |
| W590 | IBM N Line to DEC Converter | 26.00 | 282 |
| W600 | Negative Output Converter | 12.00 | 283 |
| W601 | Positive Output Converter | 13.00 | 283 |
| W602 | Bipolar Output Converter | 40.00 | 284 |
| W603 | Positive Level Amplifier | 23.00 | 161 |
| W607 | Pulse Output Converter | 42.00 | 284 |
| W640 | Pulse Output Converter | 42.00 | 284 |
| W690 | DEC to IBM N Line Converter | 36.00 | 285 |
| W700 | Switch Filter | 20.00 | 285 |
| W705 | Power Supply (3.6 Volt) | 15.00 | 285 |
| W706 | Teletype Receiver | 150.00 | 286 |
| W707 | Teletype Transmitter | 150.00 | 286 |
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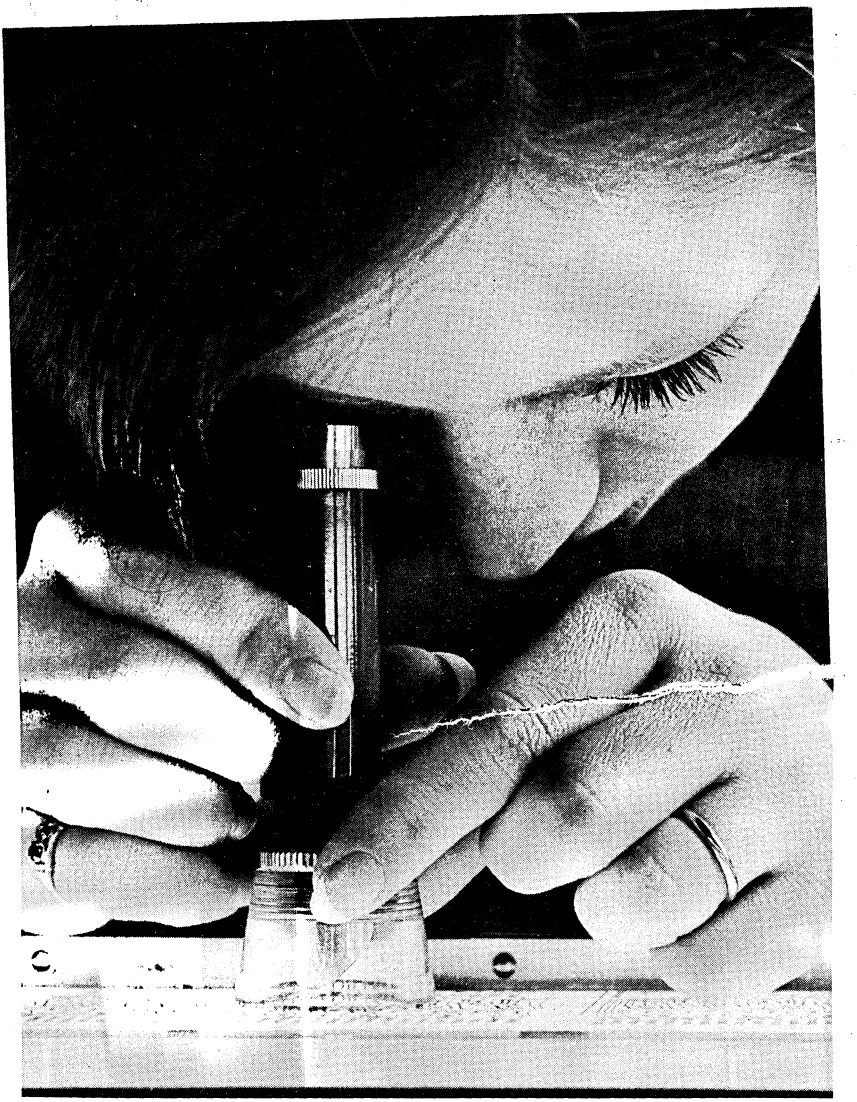

All DEC modules are exhaustively inspected and tested, both visually and electronically. A typical module undergoes a printed circuit board inspection procedure that consists of over 70 individual steps.

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